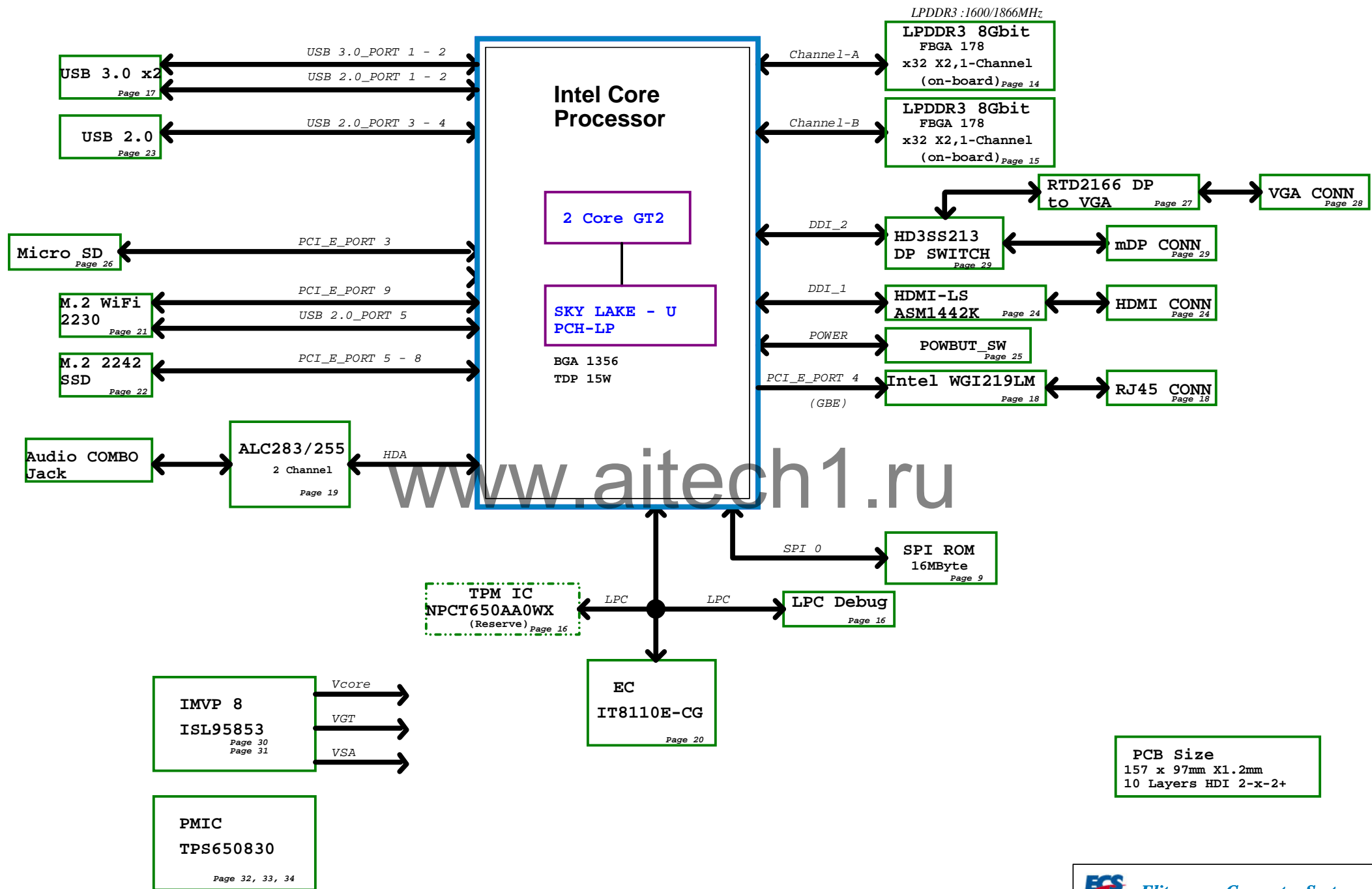




ECS
CONFIDENTIAL



PCH-GPIO function

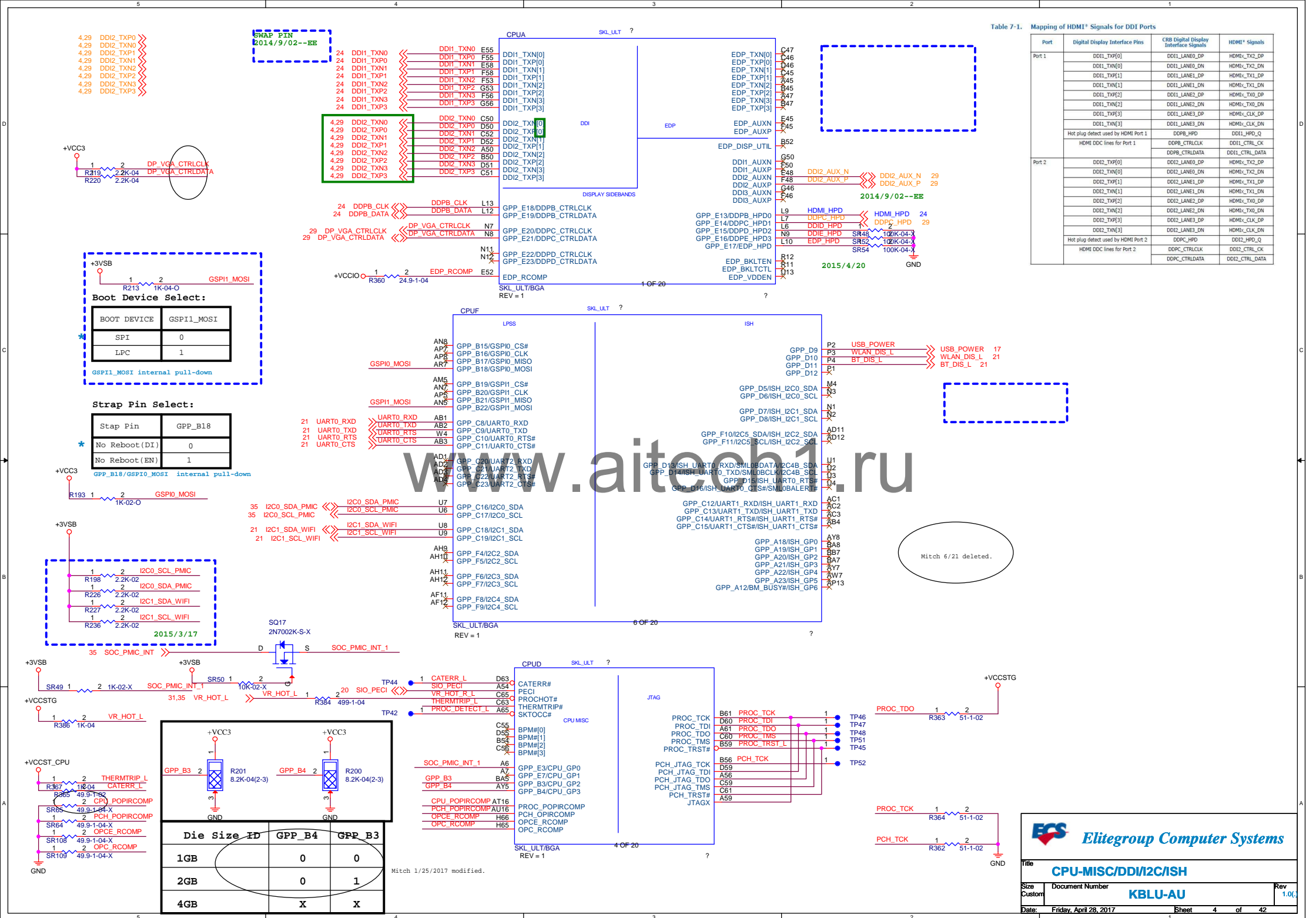
Pin Name	Power Well	Usage	Default Status
GPP_A14	3VSB	LPCPD_L	SUS_STAT#
GPP_B5	3VSB	UART_WAKE	GPI
GPP_B6	VCC3	CLKREQ1_SSD_L (PCI_E port 9 - 12)	GPI
GPP_B7	VCC3	ILAN_CLKREQ (PCI_E port 4)	GPI
GPP_B8	VCC3	CK_REQ3_L (PCI_E port 5)	GPI
GPP_B9	VCC3	CK_REQ4_L (PCI_E port 3)	GPI
GPP_B10	VCC3	CLKREQ5_L	GPI
GPP_B13	N/A	PCH_PLTRST_L	PLTRST#
GPP_B14	+VCC3	PCH_SPKR	SPKR
GPP_B3	+VCC3	MEMORY_DIE_SIZE_ID0	GPI
GPP_B4	+VCC3	MEMORY_DIE_SIZE_ID1	GPI
GPP_D0	+VCC3	MEMORY_SIZE	GPI
GPP_D1	+VCC3	MB_ID1	GPI
GPP_D2	+VCC3	MB_ID2	GPI
GPP_D3	+VCC3	MEMORY_VENDOR_ID	GPI
GPP_D9	3VSB	USB_POWER	GPO S0/S3:High, S4/S5:Low
GPP_D10	3VSB	WLAN_DIS_L	GPO S0/S3/S4/S5:High
GPP_D11	3VSB	BT_DIS_L	GPO S0/S3/S4/S5:High
GPP_D17	+VCC3	DP_VGA_HPD	GPI
GPP_D18	+VCC3	DP_HPD	GPI
GPP_D19	+VCC3	DDI2_MDP_VGA_SEL	GPO Low:MDP, Hi:VGA
GPP_D20	+VCC3	HPD_DISABLE_L	GPO Low:HDP disable, Hi:HDP enable
GPP_D21	+VCC3	A1 select	GPI For Acer Reserve
GPP_D22	+VCC3	A2 select	GPI For Acer Reserve
GPP_E1	+VCC3	SSD_DETECT_L	GPI Soft strap Dynamic select: Low/SATA, High/PCIe
GPP_E2	+VCC3	PCHEALTH_SCI_L	GPI
GPP_E3	3VSB	SOC_PMIC_INT	GPI
GPP_E4	3VSB	BIOS_WP	GPO
GPP_E5	+VCC3	DEVSLP1	GPO
GPP_E6	+VCC3	THERMAL_SD	GPI
GPD0	DSW	ILAN_WAKE_L	LAN_WAKE#
GPD10	DSW	ME_Disable	GPO
GPP_C6	3VSB	SML1_CLK	GPI
GPP_C7	3VSB	SML1_DATA	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
CRX1/WUI17/SMCLK3/GPH1(1.8)	DSW	SLP_SUS_L	GPH1(DI)
CTX1/WUI18/SMDAT3/GPH2(1.8)	+VCC3	PCHEALTH_SCI_L	GPH2(DOD)
WUI68/GPG1(1.8)	+VCC3	THERMAL_SD	GP13(DOD)
WUI37/GPC0	DSW	SLP_S4_L	GPC0(DI)
PWRSW#/GPE4	DSW	SLP_S3_L	GPE4(DI)
WUI64/GPD5	DSW	V_PON_P4_P	GPD5(DI)
CLKRUN#/WUI16/GPH0	DSW	H_PON_P14_P	GPH0(DI)
(1.8)WUI0/GPD0	DSW	V_PON_P11_P	GPD0(DI)
TACH0A/WUI65/GPD6	+VCC3	FAN_TAC1	TACH0A
PWM0/WUI43/GPA0	+VCC3	FAN_CTL1	PWM0
(1.8)SMCLK2/PECI/WUI22/GPF6	+VCC3	SIO_PECI_L	PECI
(1.8)SMCLK0/WUI55/GPB3	+3VSB	EC_SML1_CLK	SMCLK0
(1.8)SMDAT0/WUI46/GPB4	+3VSB	EC_SML1_DATA	SMDAT0
(1.8)WUI24/GPE0	+3VSB	PWR_LED0	GPE0(DOD)
(1.8)WUI7/GPE7	+3VSB	PWR_LED1	GPE7(DOD)

PCH-INT Function

Function	INT Port	PCIE_X1 Port	Device
PCIe Intel_LAN	INT A#	PE_TX/RX_3	WGI219LM
PCIe M.2(2242)	INT A#	N/A	SATA



Mitch 07/26/16 swap for NIL.

IL/NIL

CPUB

SKL_UL1

14	M_A_DQ00	M_A_DQ00	AL71	DDR0_DQ[0]
14	M_A_DQ01	M_A_DQ01	AL68	DDR0_DQ[1]
14	M_A_DQ02	M_A_DQ02	AN68	DDR0_DQ[2]
14	M_A_DQ03	M_A_DQ03	AN69	DDR0_DQ[3]
14	M_A_DQ04	M_A_DQ04	AL70	DDR0_DQ[4]
14	M_A_DQ05	M_A_DQ05	AL69	DDR0_DQ[5]
14	M_A_DQ06	M_A_DQ06	AN70	DDR0_DQ[6]
14	M_A_DQ07	M_A_DQ07	AN71	DDR0_DQ[7]
14	M_A_DQ08	M_A_DQ08	AR70	DDR0_DQ[8]
14	M_A_DQ09	M_A_DQ09	AR68	DDR0_DQ[9]
14	M_A_DQ10	M_A_DQ10	AU71	DDR0_DQ[10]
14	M_A_DQ11	M_A_DQ11	AU68	DDR0_DQ[11]
14	M_A_DQ12	M_A_DQ12	AR71	DDR0_DQ[12]
14	M_A_DQ13	M_A_DQ13	AR69	DDR0_DQ[13]
14	M_A_DQ14	M_A_DQ14	AU70	DDR0_DQ[14]
14	M_A_DQ15	M_A_DQ15	AU69	DDR0_DQ[15]
14	M_A_DQ32	M_A_DQ32	B855	DDR0_DQ[16]/DDR0_DQ[32]
14	M_A_DQ33	M_A_DQ33	AW65	DDR0_DQ[17]/DDR0_DQ[33]
14	M_A_DQ34	M_A_DQ34	AW63	DDR0_DQ[18]/DDR0_DQ[34]
14	M_A_DQ35	M_A_DQ35	AY63	DDR0_DQ[19]/DDR0_DQ[35]
14	M_A_DQ36	M_A_DQ36	BA65	DDR0_DQ[20]/DDR0_DQ[36]
14	M_A_DQ37	M_A_DQ37	AY65	DDR0_DQ[21]/DDR0_DQ[37]
14	M_A_DQ38	M_A_DQ38	BA63	DDR0_DQ[22]/DDR0_DQ[38]
14	M_A_DQ39	M_A_DQ39	B863	DDR0_DQ[23]/DDR0_DQ[39]
14	M_A_DQ40	M_A_DQ40	BA61	DDR0_DQ[24]/DDR0_DQ[40]
14	M_A_DQ41	M_A_DQ41	AW61	DDR0_DQ[25]/DDR0_DQ[41]
14	M_A_DQ42	M_A_DQ42	B859	DDR0_DQ[26]/DDR0_DQ[42]
14	M_A_DQ43	M_A_DQ43	AW59	DDR0_DQ[27]/DDR0_DQ[43]
14	M_A_DQ44	M_A_DQ44	B861	DDR0_DQ[28]/DDR0_DQ[44]
14	M_A_DQ45	M_A_DQ45	AY61	DDR0_DQ[29]/DDR0_DQ[45]
14	M_A_DQ46	M_A_DQ46	BA59	DDR0_DQ[30]/DDR0_DQ[46]
14	M_A_DQ47	M_A_DQ47	AY59	DDR0_DQ[31]/DDR0_DQ[47]
15	M_B_DQ00	M_B_DQ00	AY39	DDR0_DQ[32]/DDR1_DQ[0]
15	M_B_DQ01	M_B_DQ01	AW39	DDR0_DQ[33]/DDR1_DQ[1]
15	M_B_DQ02	M_B_DQ02	AY37	DDR0_DQ[34]/DDR1_DQ[2]
15	M_B_DQ03	M_B_DQ03	AW37	DDR0_DQ[35]/DDR1_DQ[3]
15	M_B_DQ04	M_B_DQ04	B839	DDR0_DQ[36]/DDR1_DQ[4]
15	M_B_DQ05	M_B_DQ05	BA39	DDR0_DQ[37]/DDR1_DQ[5]
15	M_B_DQ06	M_B_DQ06	BA37	DDR0_DQ[38]/DDR1_DQ[6]
15	M_B_DQ07	M_B_DQ07	B837	DDR0_DQ[39]/DDR1_DQ[7]
15	M_B_DQ08	M_B_DQ08	AY35	DDR0_DQ[40]/DDR1_DQ[8]
15	M_B_DQ09	M_B_DQ09	AW35	DDR0_DQ[41]/DDR1_DQ[9]
15	M_B_DQ10	M_B_DQ10	AY33	DDR0_DQ[42]/DDR1_DQ[10]
15	M_B_DQ11	M_B_DQ11	AW33	DDR0_DQ[43]/DDR1_DQ[11]
15	M_B_DQ12	M_B_DQ12	B835	DDR0_DQ[44]/DDR1_DQ[12]
15	M_B_DQ13	M_B_DQ13	BA35	DDR0_DQ[45]/DDR1_DQ[13]
15	M_B_DQ14	M_B_DQ14	B833	DDR0_DQ[46]/DDR1_DQ[14]
15	M_B_DQ15	M_B_DQ15	AY31	DDR0_DQ[47]/DDR1_DQ[15]
15	M_B_DQ32	M_B_DQ32	AY31	DDR0_DQ[48]/DDR1_DQ[32]
15	M_B_DQ33	M_B_DQ33	AW31	DDR0_DQ[49]/DDR1_DQ[33]
15	M_B_DQ34	M_B_DQ34	AY29	DDR0_DQ[50]/DDR1_DQ[34]
15	M_B_DQ35	M_B_DQ35	AW29	DDR0_DQ[51]/DDR1_DQ[35]
15	M_B_DQ36	M_B_DQ36	B831	DDR0_DQ[52]/DDR1_DQ[36]
15	M_B_DQ37	M_B_DQ37	BA31	DDR0_DQ[53]/DDR1_DQ[37]
15	M_B_DQ38	M_B_DQ38	BA29	DDR0_DQ[54]/DDR1_DQ[38]
15	M_B_DQ39	M_B_DQ39	B829	DDR0_DQ[55]/DDR1_DQ[39]
15	M_B_DQ40	M_B_DQ40	AY27	DDR0_DQ[56]/DDR1_DQ[40]
15	M_B_DQ41	M_B_DQ41	AW27	DDR0_DQ[57]/DDR1_DQ[41]
15	M_B_DQ42	M_B_DQ42	AY25	DDR0_DQ[58]/DDR1_DQ[42]
15	M_B_DQ43	M_B_DQ43	AW25	DDR0_DQ[59]/DDR1_DQ[43]
15	M_B_DQ44	M_B_DQ44	B827	DDR0_DQ[60]/DDR1_DQ[44]
15	M_B_DQ45	M_B_DQ45	BA27	DDR0_DQ[61]/DDR1_DQ[45]
15	M_B_DQ46	M_B_DQ46	BA25	DDR0_DQ[62]/DDR1_DQ[46]
15	M_B_DQ47	M_B_DQ47	B825	DDR0_DQ[63]/DDR1_DQ[47]

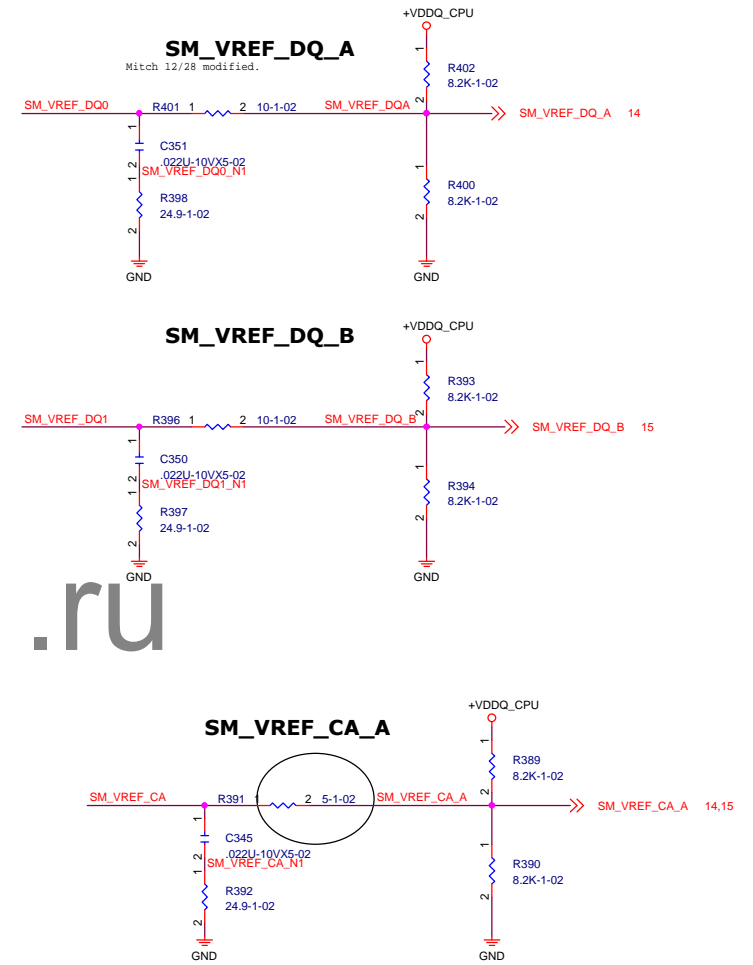
DDR0_CKN[0]	AU53	M_CLK_A_N0	14
DDR0_CKP[0]	AT53	M_CLK_A_P0	14
DDR0_CKN[1]	AU55	M_CLK_A_N1	14
DDR0_CKP[1]	AT55	M_CLK_A_P1	14
DDR0_CKE[0]	BA56	M_CKE_A0	14
DDR0_CKE[1]	B856	M_CKE_A1	14
DDR0_CKE[2]	AW56	M_CKE_A2	14
DDR0_CKE[3]	AY56	M_CKE_A3	14
DDR0_CS[0]	AU45	M_CS_A_L0	14
DDR0_CS[1]	AT45	M_CS_A_L1	14
DDR0_ODT[0]	AT43	M_ODT_A	14
DDR0_ODT[1]	AT43	M_ODT_A	14
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BA51	M_A_CAA0	14
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	B854	M_A_CAA1	14
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	BA52	M_A_CAA2	14
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AY52	M_A_CAA3	14
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AW52	M_A_CAA4	14
DDR0_MA[2]/DDR0_CAA[5]/DDR0_MA[2]	AY55	M_A_CAA5	14
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	AW54	M_A_CAA6	14
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA54	M_A_CAA7	14
DDR0_MA[15]/DDR0_CAA[8]/DDR0_MA[15]	BA55	M_A_CAA8	14
DDR0_MA[14]/DDR0_CAA[9]/DDR0_MA[14]	AY54	M_A_CAA9	14
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU46	M_A_CAB0	14
DDR0_CAS[0]/DDR0_CAB[1]/DDR0_MA[15]	AU48	M_A_CAB1	14
DDR0_WE[0]/DDR0_CAB[2]/DDR0_MA[14]	AT46	M_A_CAB2	14
DDR0_RAS[0]/DDR0_CAB[3]/DDR0_MA[16]	AU50	M_A_CAB3	14
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AU52	M_A_CAB4	14
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AY51	M_A_CAB5	14
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT48	M_A_CAB6	14
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	AT50	M_A_CAB7	14
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	B850	M_A_CAB8	14
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AY50	M_A_CAB9	14
DDR0_MA[3]	BA50	M_A_CAB9	14
DDR0_MA[4]	B852	M_A_CAB9	14
DDR0_DQSN[0]	AM70	M_DQS_A_N0	14
DDR0_DQSP[0]	AM69	M_DQS_A_P0	14
DDR0_DQSN[1]	AT69	M_DQS_A_N1	14
DDR0_DQSP[1]	AT69	M_DQS_A_P1	14
DDR0_DQSN[2]	BA64	M_DQS_A_N4	14
DDR0_DQSP[2]	BA64	M_DQS_A_P4	14
DDR0_DQSN[3]	AY60	M_DQS_A_N5	14
DDR0_DQSP[3]	BA60	M_DQS_A_P5	14
DDR0_DQSN[4]	BA38	M_DQS_B_N0	15
DDR0_DQSP[4]	AY38	M_DQS_B_P0	15
DDR0_DQSN[5]	AY34	M_DQS_B_N1	15
DDR0_DQSP[5]	BA34	M_DQS_B_P1	15
DDR0_DQSN[6]	BA30	M_DQS_B_N4	15
DDR0_DQSP[6]	AY30	M_DQS_B_P4	15
DDR0_DQSN[7]	AY26	M_DQS_B_N5	15
DDR0_DQSP[7]	BA26	M_DQS_B_P5	15
DDR0_ALERT#	AW50	SR90	2
DDR0_PAR	AT52	0-02-X	
DDR_VREF_CA	AY67	SM_VREF_CA	
DDR0_VREF_DQ	AY68	SM_VREF_DQ0	
DDR1_VREF_DQ	BA67	SM_VREF_DQ1	
DDR_VTT_CTRL	AW67	DDR_VTT_CTRL	35

DDR CH - A

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SKL_UL1/BGA
REV = 1

Place part of REF circuit near LPDDR3 chips.



Mitch 07/26/18 swap for NIL.

14	M.A.DQ16	M.A.DQ16	AF65
14	M.A.DQ17	M.A.DQ17	AF64
14	M.A.DQ18	M.A.DQ18	AK65
14	M.A.DQ19	M.A.DQ19	AK64
14	M.A.DQ20	M.A.DQ20	AF66
14	M.A.DQ21	M.A.DQ21	AF67
14	M.A.DQ22	M.A.DQ22	AK67
14	M.A.DQ23	M.A.DQ23	AK66
14	M.A.DQ24	M.A.DQ24	AF70
14	M.A.DQ25	M.A.DQ25	AF68
14	M.A.DQ26	M.A.DQ26	AH71
14	M.A.DQ27	M.A.DQ27	AH68
14	M.A.DQ28	M.A.DQ28	AF71
14	M.A.DQ29	M.A.DQ29	AF69
14	M.A.DQ30	M.A.DQ30	AH70
14	M.A.DQ31	M.A.DQ31	AH69
14	M.A.DQ32	M.A.DQ32	AT66
14	M.A.DQ33	M.A.DQ33	AU66
14	M.A.DQ34	M.A.DQ34	AP65
14	M.A.DQ35	M.A.DQ35	AN65
14	M.A.DQ36	M.A.DQ36	AN66
14	M.A.DQ37	M.A.DQ37	AP66
14	M.A.DQ38	M.A.DQ38	AT65
14	M.A.DQ39	M.A.DQ39	AU65
14	M.A.DQ40	M.A.DQ40	AT61
14	M.A.DQ41	M.A.DQ41	AU61
14	M.A.DQ42	M.A.DQ42	AP60
14	M.A.DQ43	M.A.DQ43	AN60
14	M.A.DQ44	M.A.DQ44	AN61
14	M.A.DQ45	M.A.DQ45	AP61
14	M.A.DQ46	M.A.DQ46	AT60
14	M.A.DQ47	M.A.DQ47	AU60
14	M.B.DQ16	M.B.DQ16	AU40
14	M.B.DQ17	M.B.DQ17	AT40
14	M.B.DQ18	M.B.DQ18	AT37
14	M.B.DQ19	M.B.DQ19	AU37
14	M.B.DQ20	M.B.DQ20	AR40
14	M.B.DQ21	M.B.DQ21	AP40
14	M.B.DQ22	M.B.DQ22	AP37
14	M.B.DQ23	M.B.DQ23	AR37
14	M.B.DQ24	M.B.DQ24	AT33
14	M.B.DQ25	M.B.DQ25	AU33
14	M.B.DQ26	M.B.DQ26	AT30
14	M.B.DQ27	M.B.DQ27	AR33
14	M.B.DQ28	M.B.DQ28	AP33
14	M.B.DQ29	M.B.DQ29	AR30
14	M.B.DQ30	M.B.DQ30	AP30
14	M.B.DQ31	M.B.DQ31	AU27
14	M.B.DQ32	M.B.DQ32	AT27
14	M.B.DQ33	M.B.DQ33	AT25
14	M.B.DQ34	M.B.DQ34	AU25
14	M.B.DQ35	M.B.DQ35	AP27
14	M.B.DQ36	M.B.DQ36	AN27
14	M.B.DQ37	M.B.DQ37	AN25
14	M.B.DQ38	M.B.DQ38	AP25
14	M.B.DQ39	M.B.DQ39	AT22
14	M.B.DQ40	M.B.DQ40	AU22
14	M.B.DQ41	M.B.DQ41	AT21
14	M.B.DQ42	M.B.DQ42	AN22
14	M.B.DQ43	M.B.DQ43	AP22
14	M.B.DQ44	M.B.DQ44	AN21

IL/NIL

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SKL_ULTBGA

REV = 1

DDR CH - B

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DDR1_CKN[0]
DDR1_CKN[1]
DDR1_CKP[0]
DDR1_CKP[1]

DDR1_CKE[0]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]

DDR1_CS#0
DDR1_CS#1
DDR1_ODT[0]
DDR1_ODT[1]

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[1]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[2]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[4]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAA[5]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[6]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[7]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAA[8]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAA[9]/DDR1_MA[14]

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAB[1]/DDR1_MA[14]
DDR1_MA[15]/DDR1_CAB[2]/DDR1_MA[15]
DDR1_MA[16]/DDR1_CAB[3]/DDR1_MA[16]
DDR1_MA[17]/DDR1_CAB[4]/DDR1_MA[17]
DDR1_MA[18]/DDR1_CAB[5]/DDR1_MA[18]
DDR1_MA[19]/DDR1_CAB[6]/DDR1_MA[19]
DDR1_MA[20]/DDR1_CAB[7]/DDR1_MA[20]
DDR1_MA[21]/DDR1_CAB[8]/DDR1_MA[21]
DDR1_MA[22]/DDR1_CAB[9]/DDR1_MA[22]

DDR1_DQS[0]/DDR1_DQS[0]
DDR1_DQS[1]/DDR1_DQS[1]
DDR1_DQS[2]/DDR1_DQS[2]
DDR1_DQS[3]/DDR1_DQS[3]
DDR1_DQS[4]/DDR1_DQS[4]
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DDR1_DQS[6]/DDR1_DQS[6]
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DDR1_ALERT#

DDR1_PAR

DRAM_RESET#

DDR1_RCOMP[0]

DDR1_RCOMP[1]

DDR1_RCOMP[2]

AN45
AN46
AP45
AP46

AN56
AN57
AN58
AN59

BB42
AY42
BA42
AW42

AY48
AP50
BA48
BB48
AP48
AP52
AN50
AN48
AN53
AN52

BA43
AY43
AY44
AR44
BB44
AY47
BA44
AW46
AY46
BA46
BA47

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AR65
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AR61
AR60
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AR38
AT32
AR32
AR25
AR27
AR22
AR21

AN43

AT13

AR18

AT18

AU18

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M.CLK_B_N1 15
M.CLK_B_P0 15
M.CLK_B_P1 15

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M.CKE_B1 15
M.CKE_B2 15
M.CKE_B3 15

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M_CS_B_L1 15
M_ODT_B 15

M_B_CAA0 15
M_B_CAA1 15
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M_B_CAA3 15
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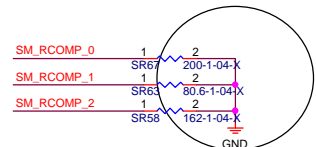
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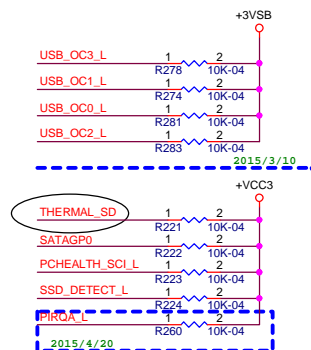
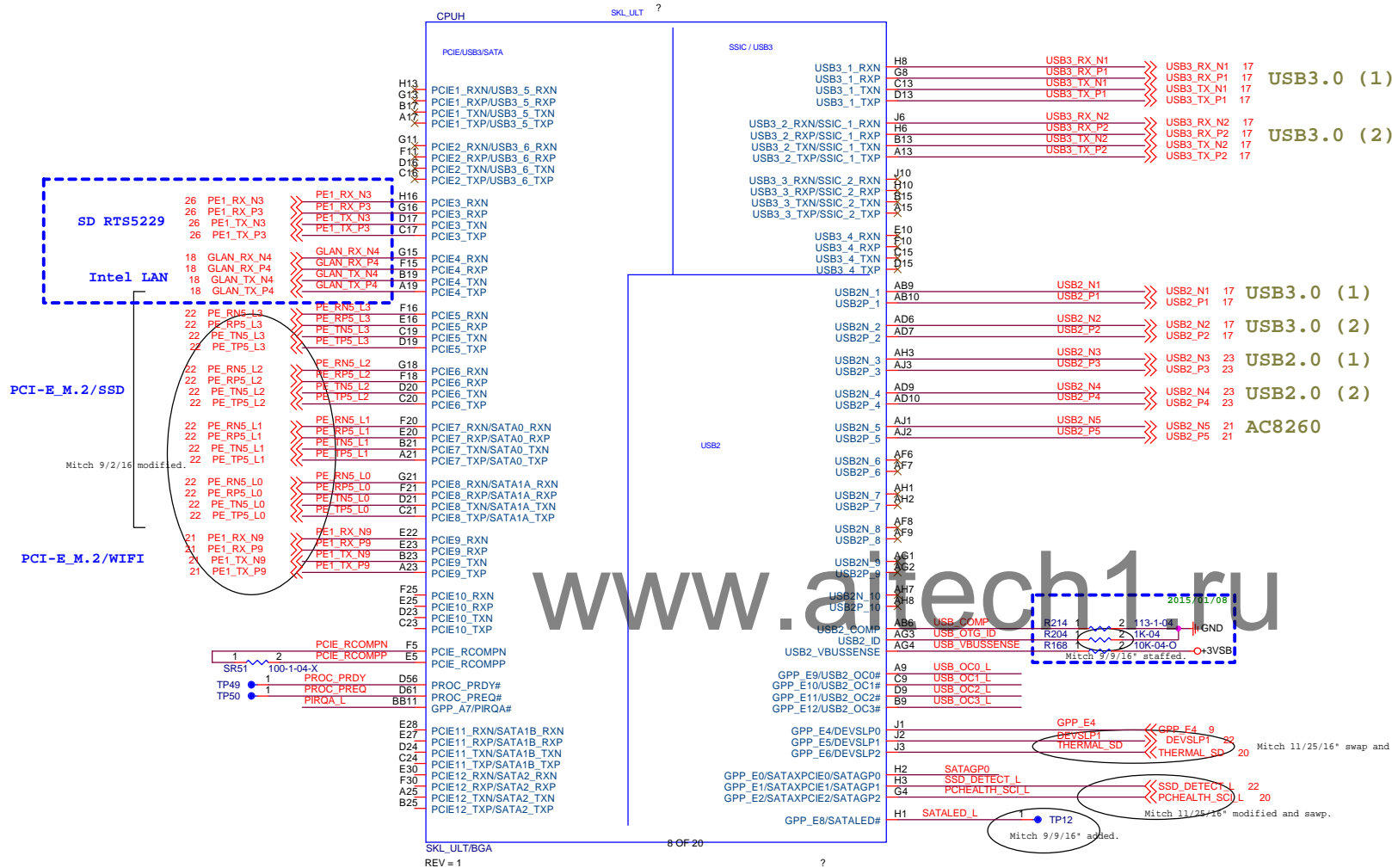
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M_DQS_A_N7 14
M_DQS_A_P7 14
M_DQS_B_N2 15
M_DQS_B_P2 15
M_DQS_B_N3 15
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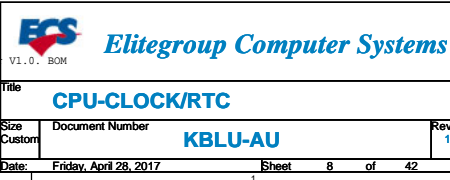
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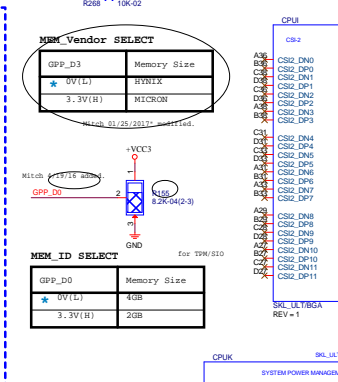
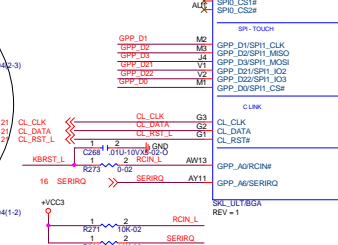
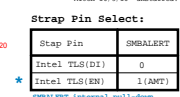
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GND

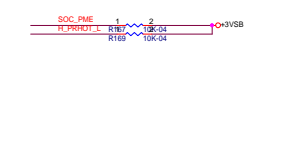
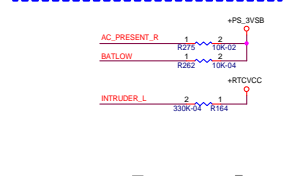
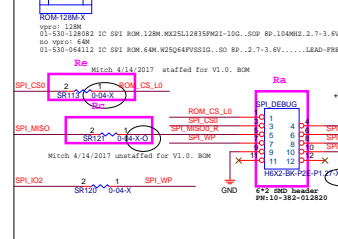
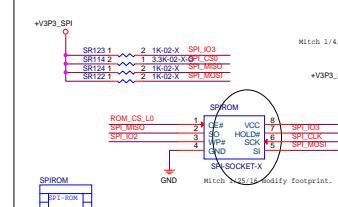
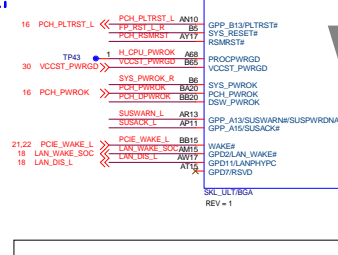




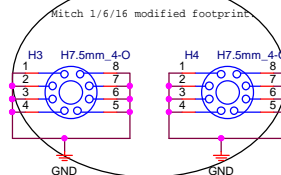
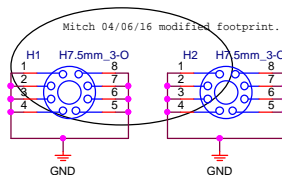
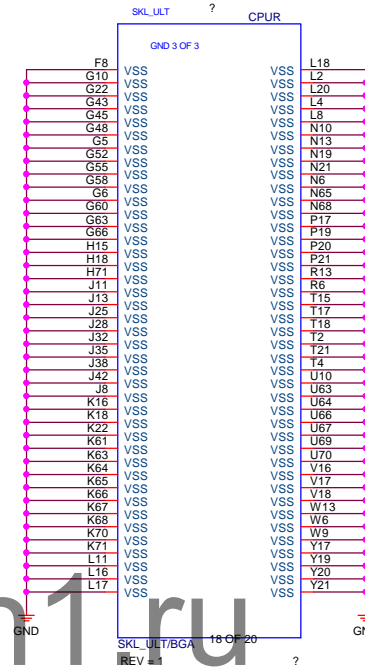
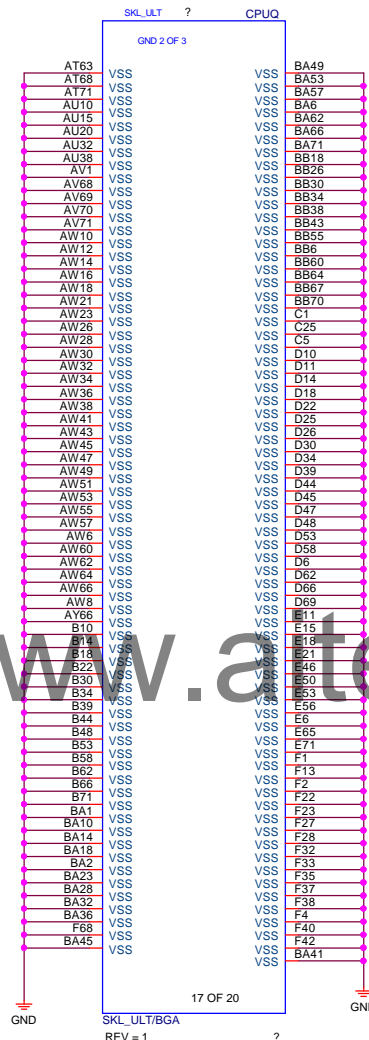
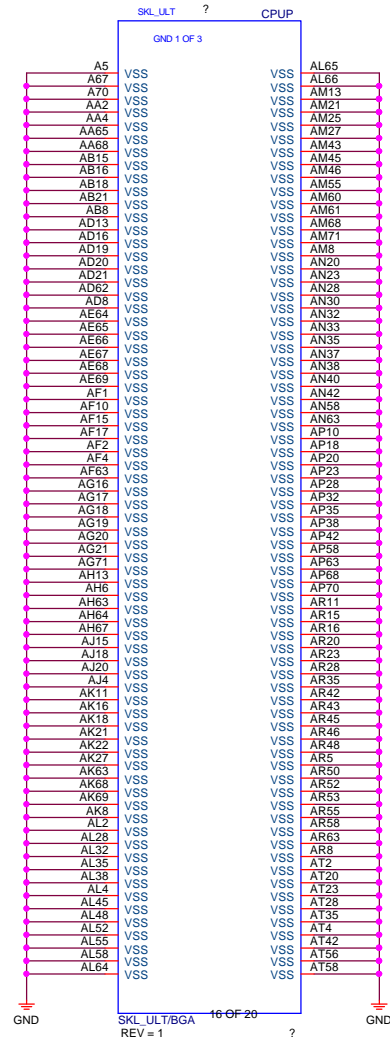


SP
SP
SP
SP
SP
SP

MEM_ID SELECT		GND	for TSM/SIO
GPP_D0	Memory Size		
* 0V(L)	4GB		
3.3V(H)	2GB		



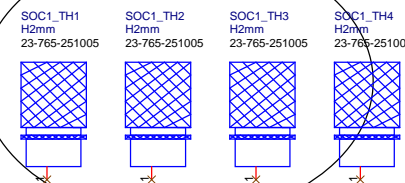
	Ra	Rb	Rc	Rd	Re
A3~A5	O	O	O	O	X
MP	X	X	X	X	O



Mitch 4/12/16 deleted.

Mitch 8/25/16 deleted.

CPU BOSS for CPU Heat Sink



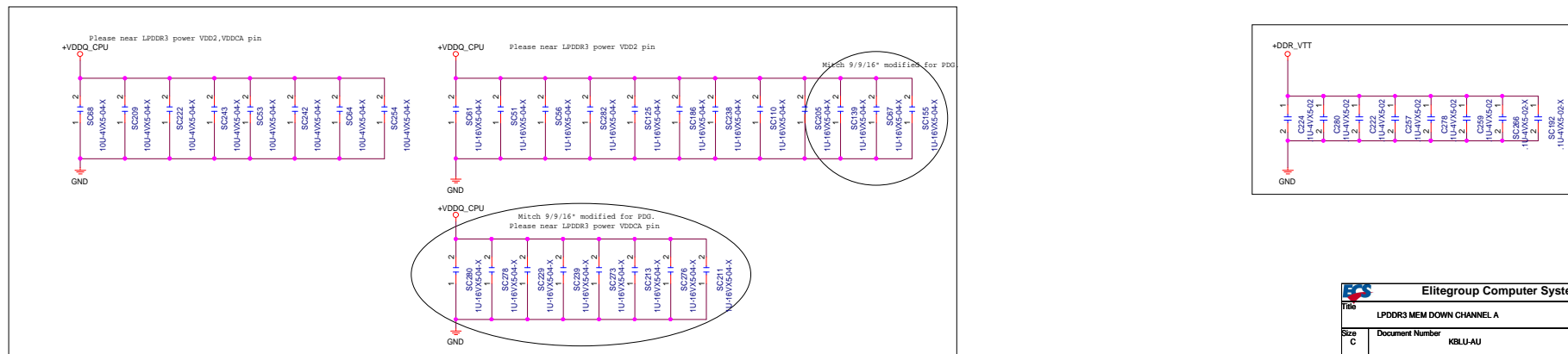
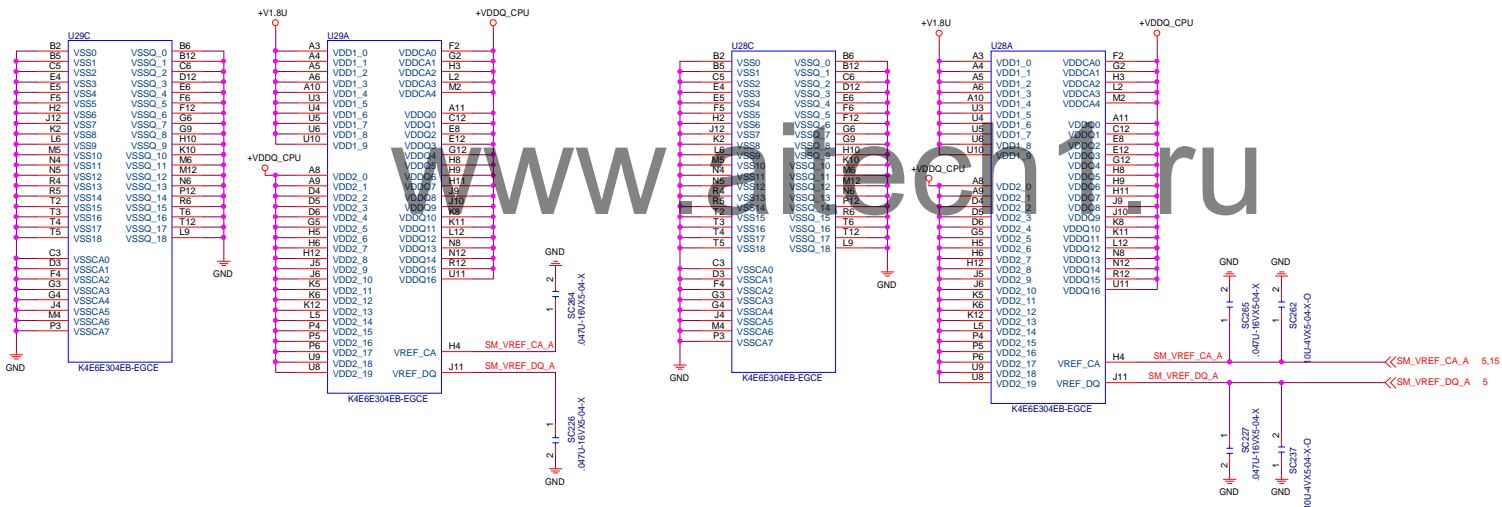
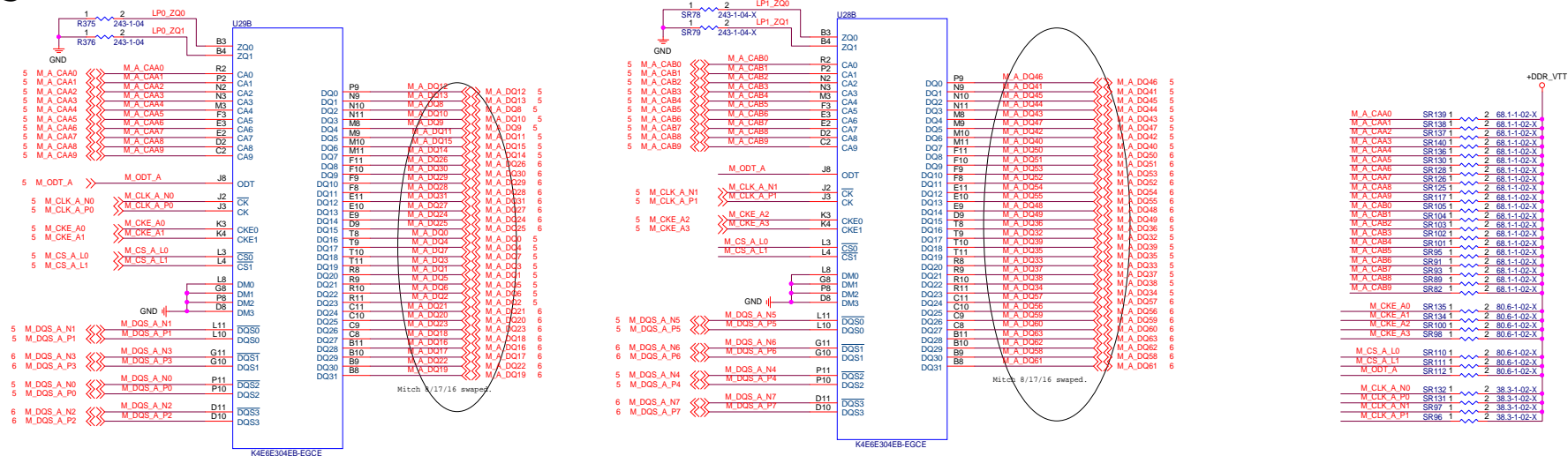
Elitegroup Computer Systems

Title: **CPU-GND**

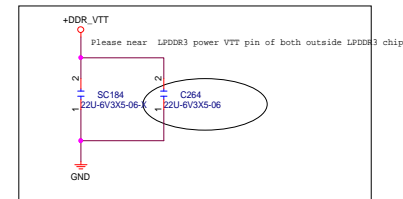
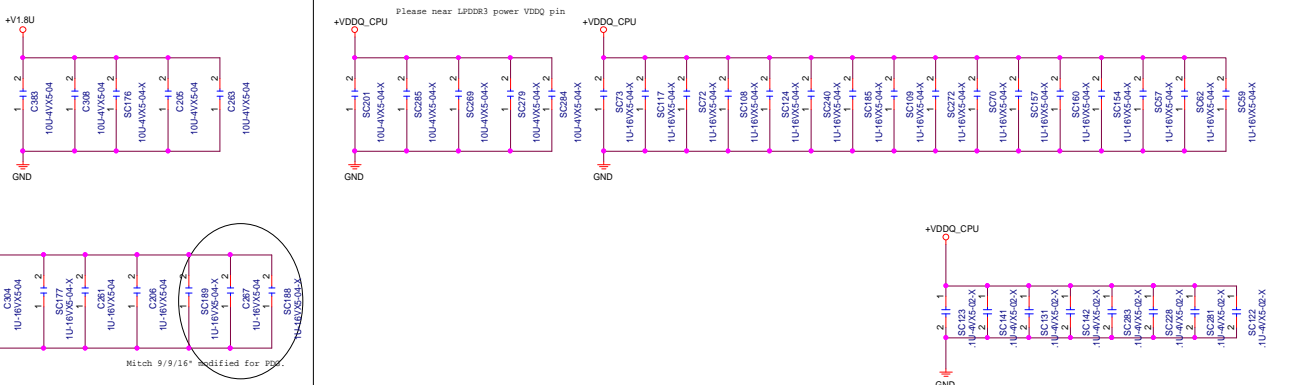
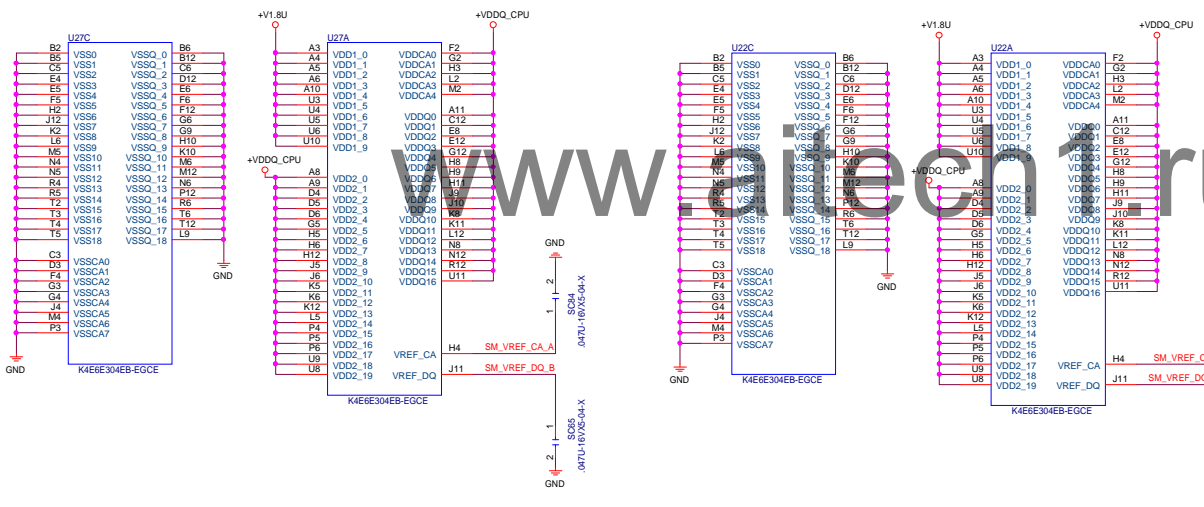
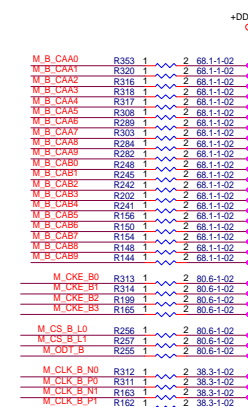
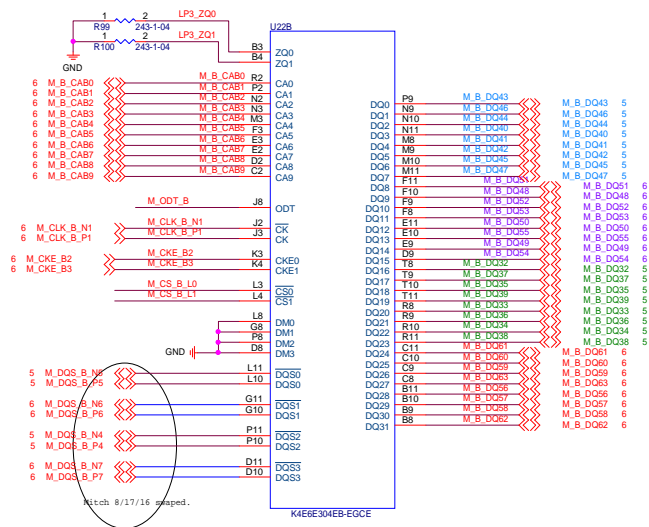
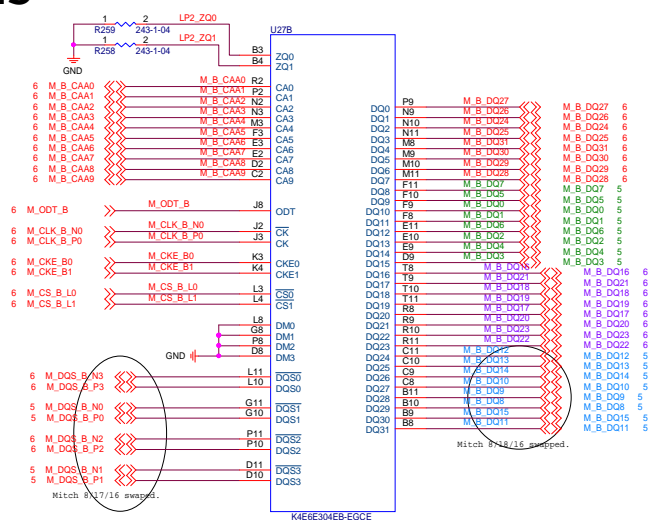
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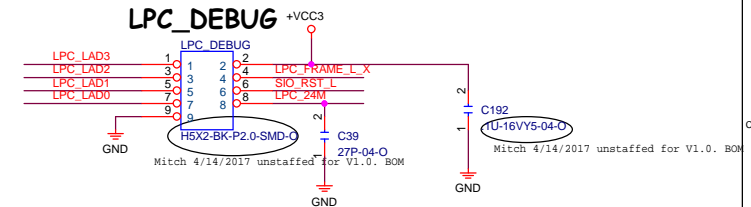
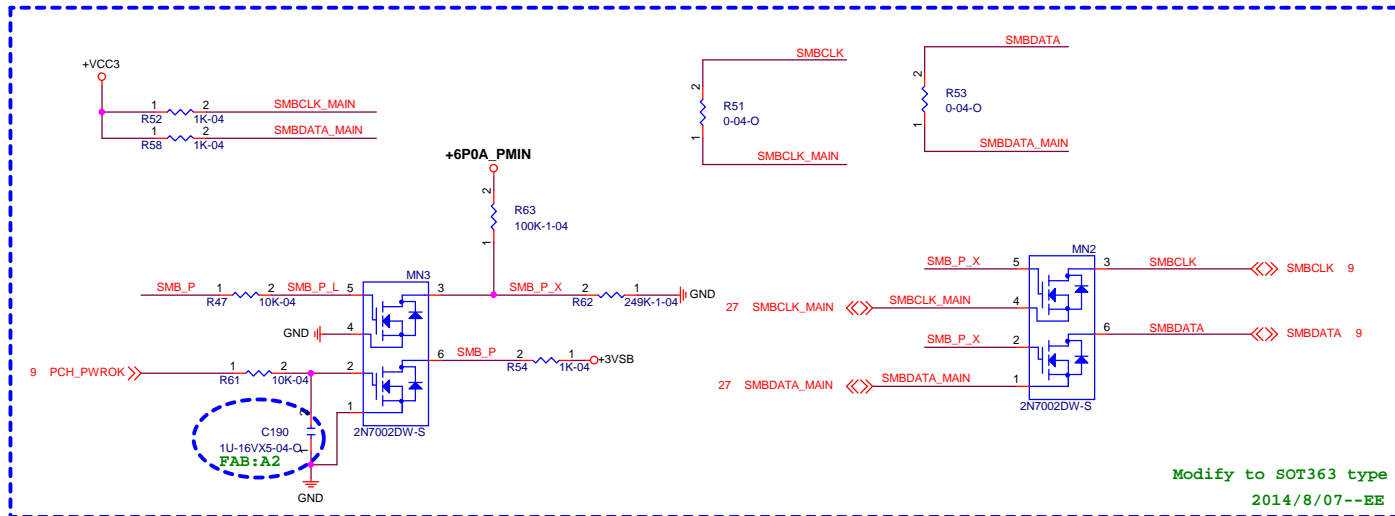
Date: Friday, April 28, 2017 Sheet: 13 of 42

LPDDR3

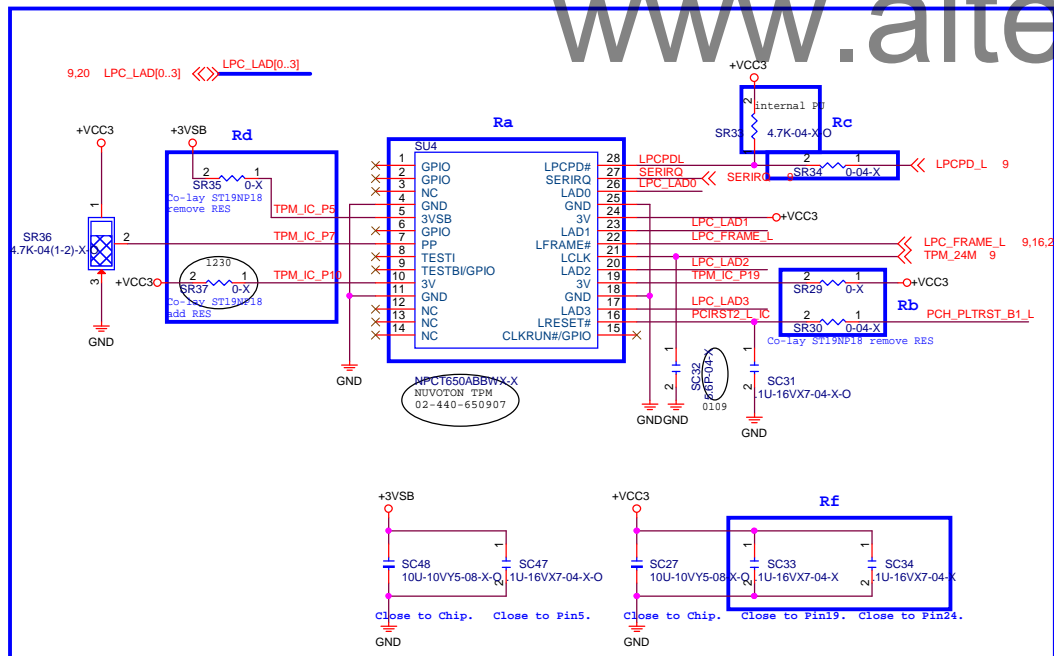
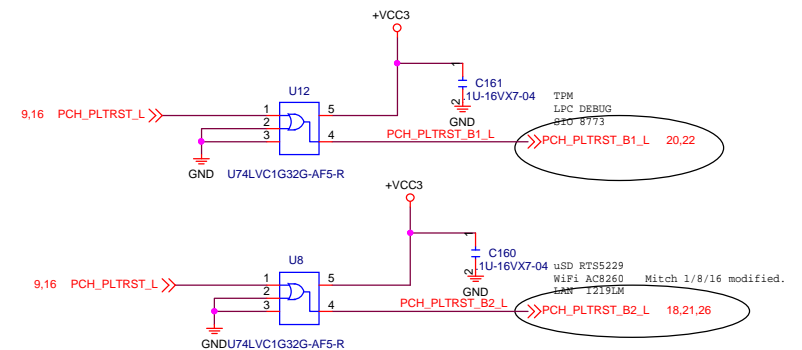
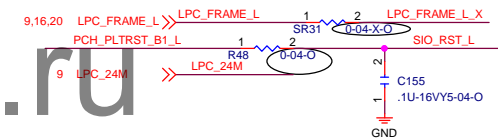


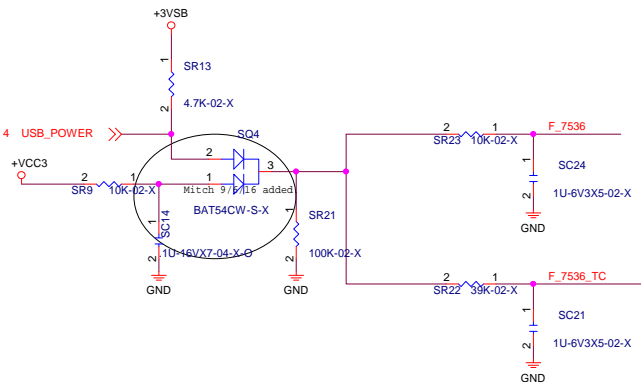
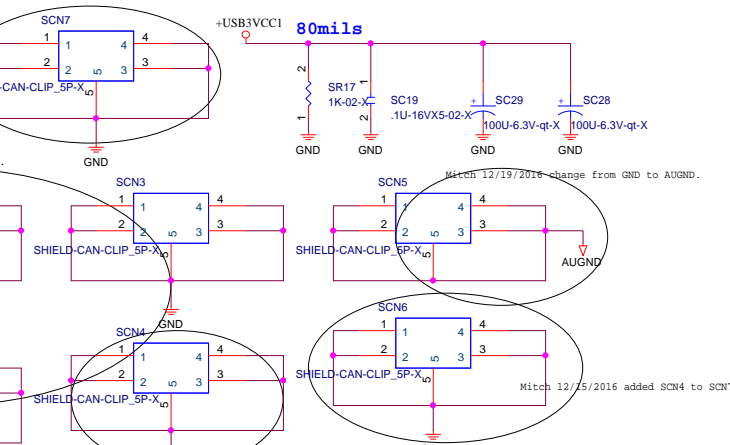
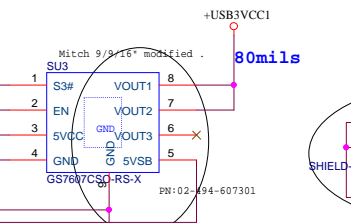
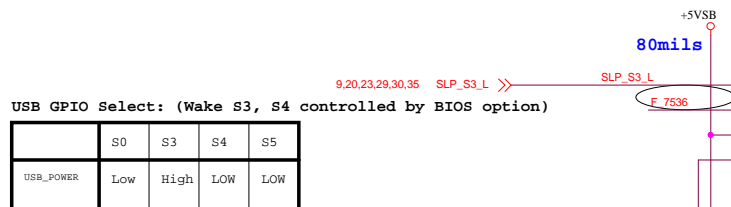
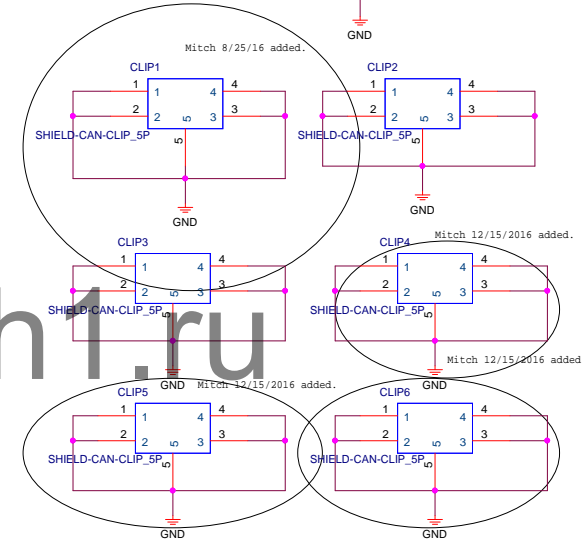
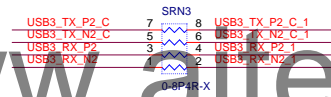
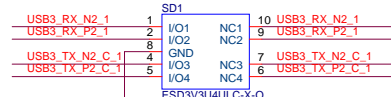
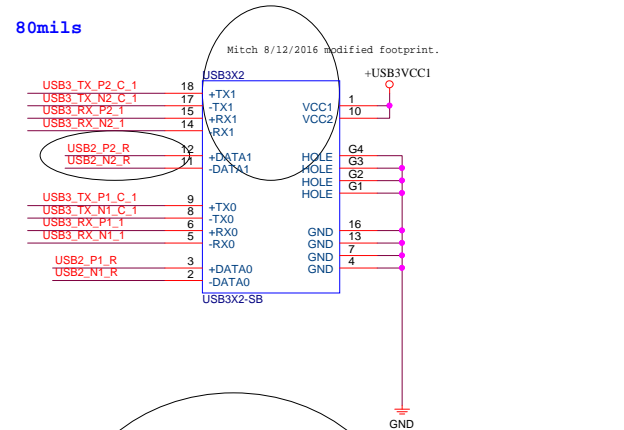
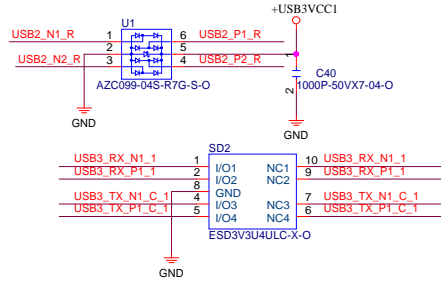
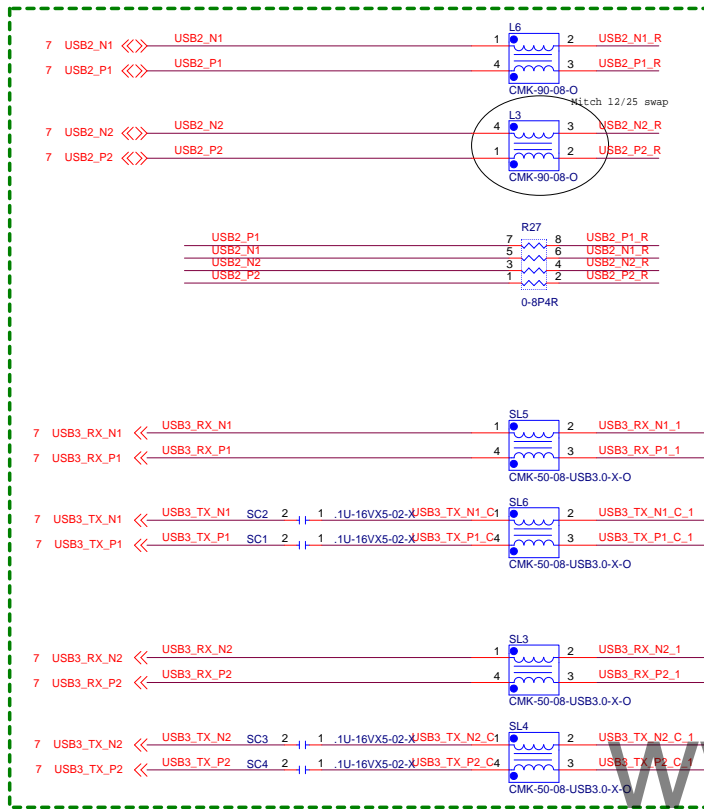
LPDDR3

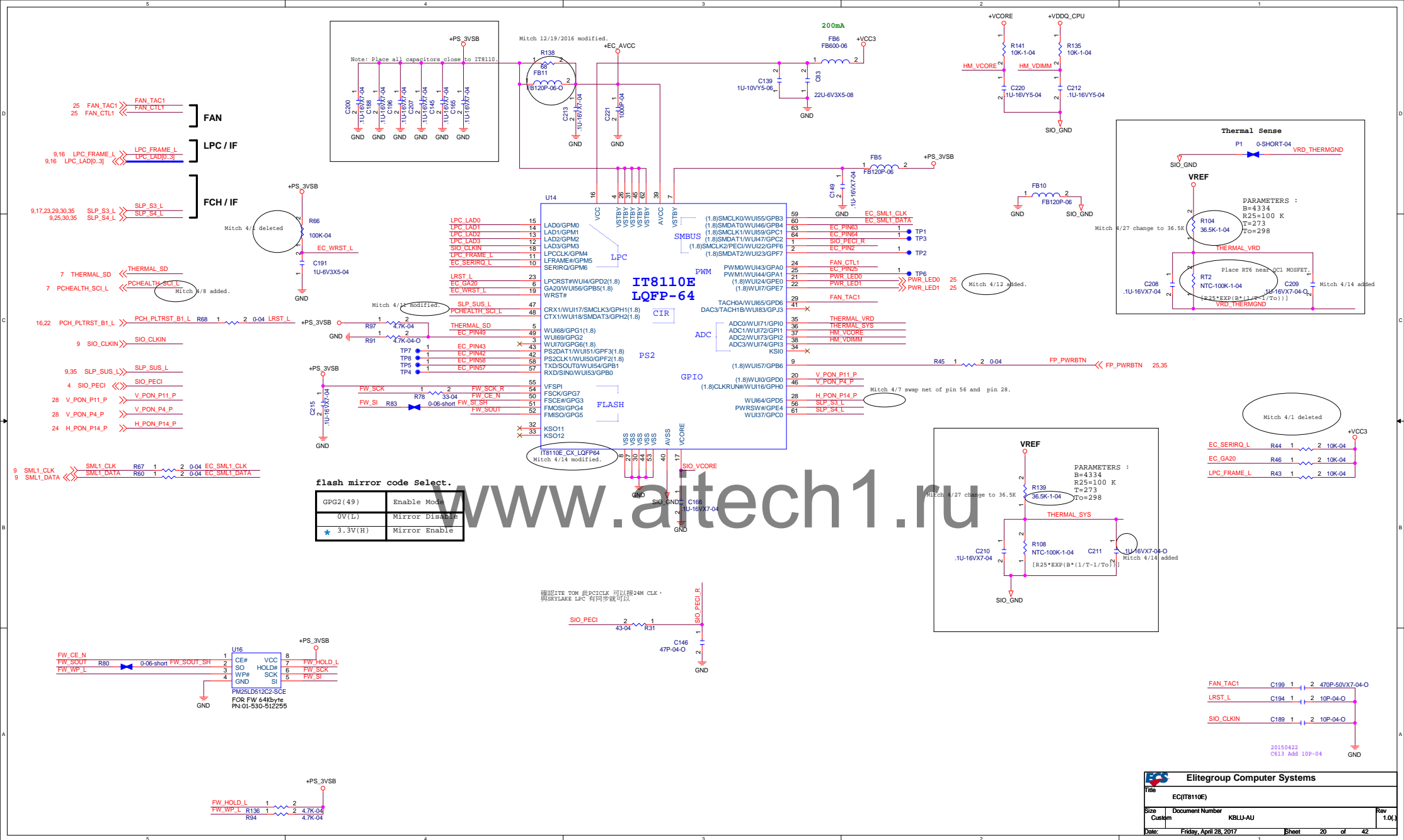


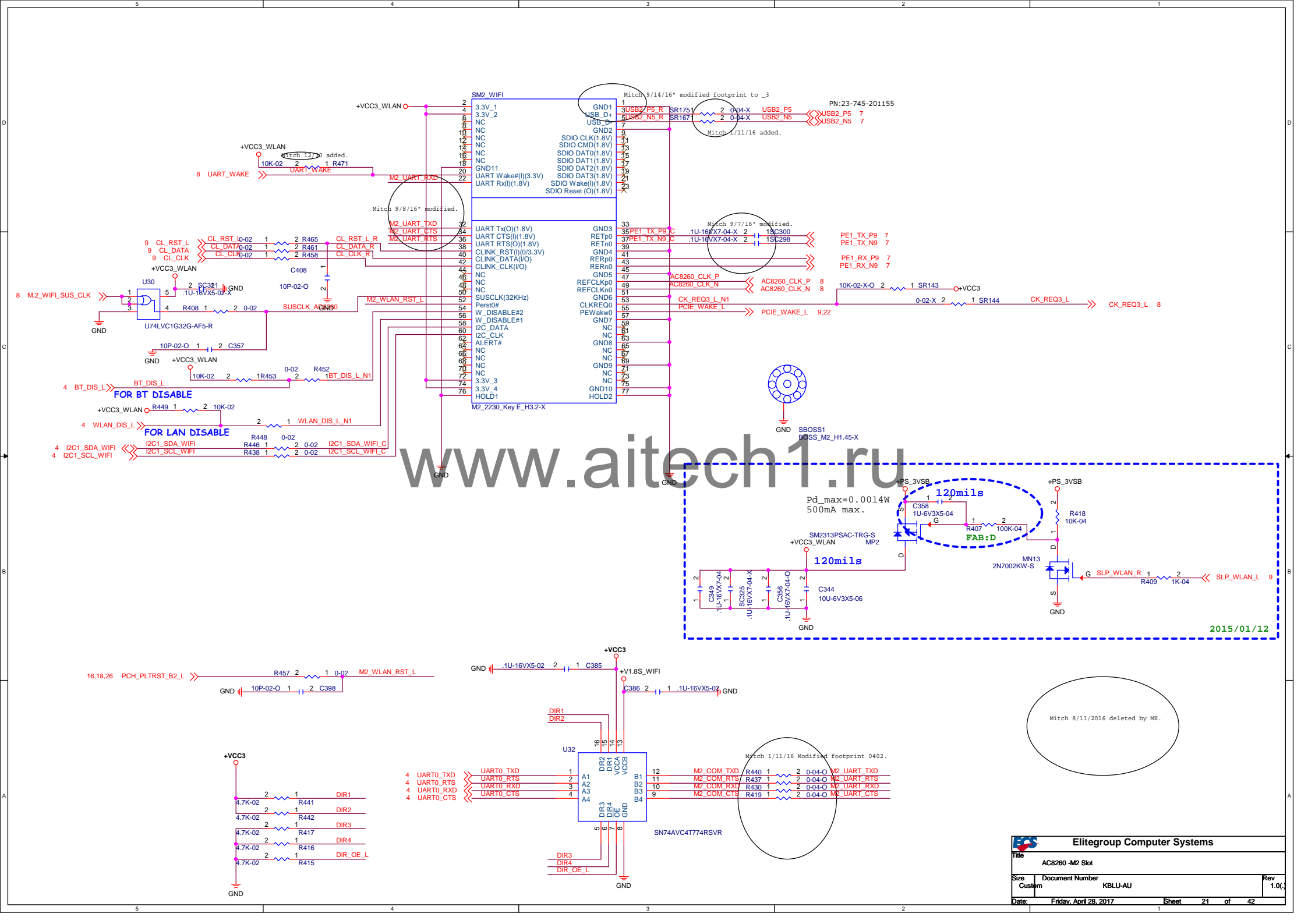


Mitch 4/14/2017 unstaffed for V1.0. BOM




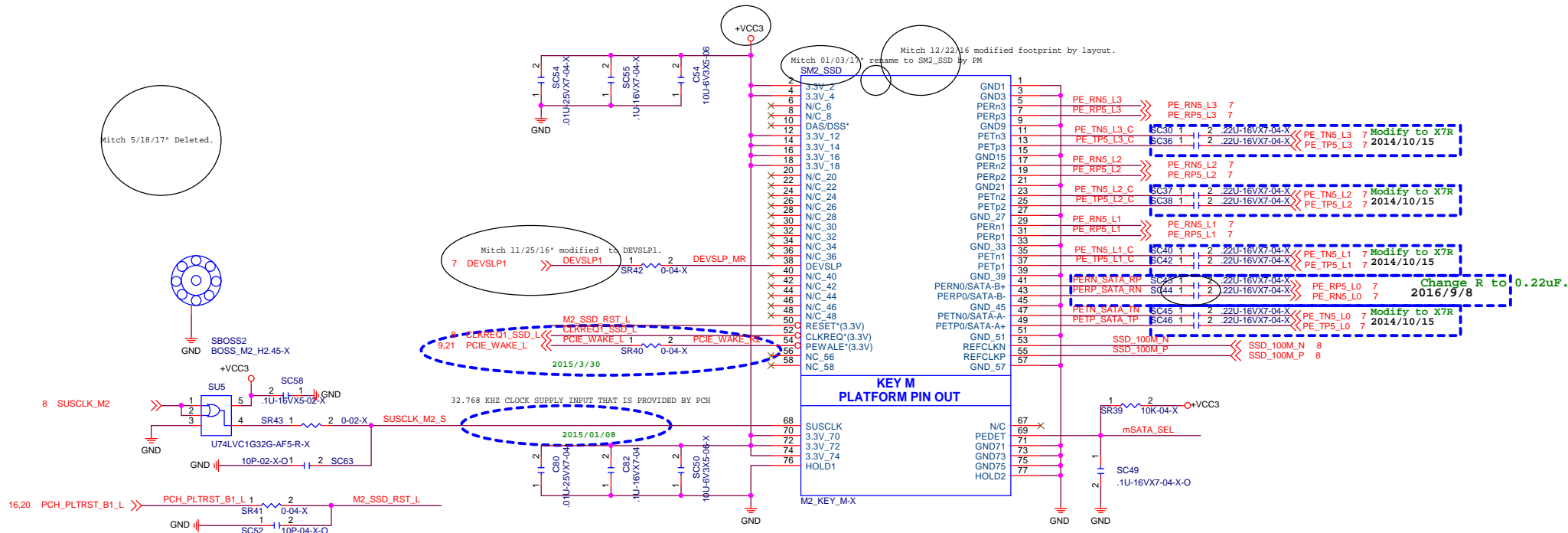




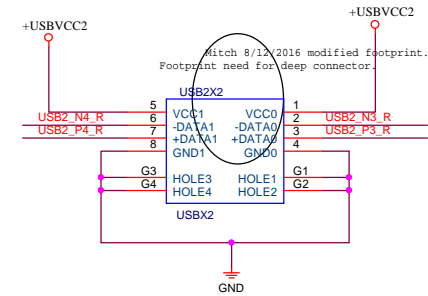
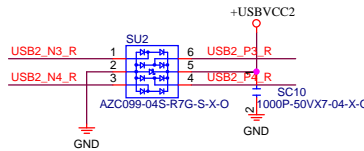
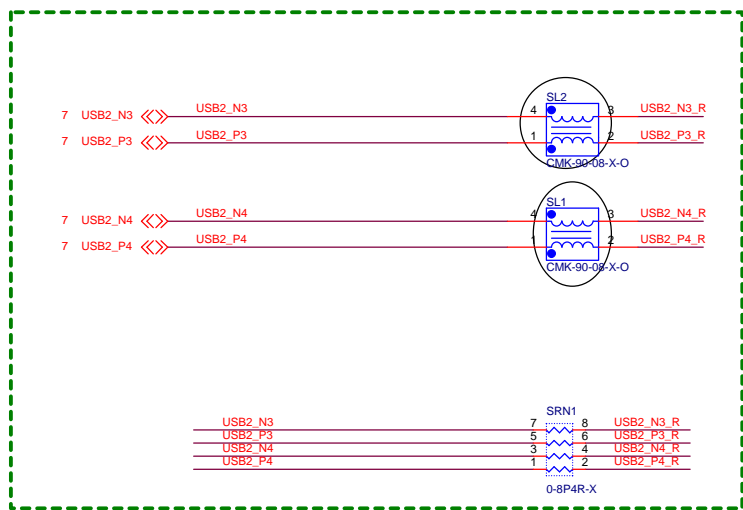


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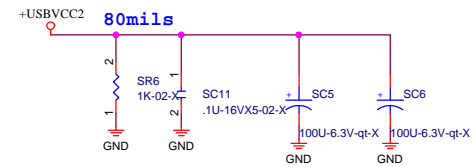
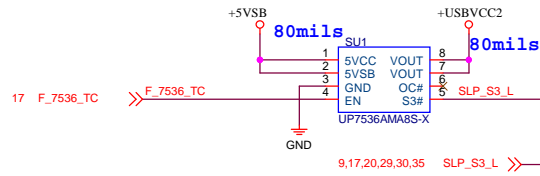
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Title			
AC8260 -M2 Slot			
Size	Document Number		Rev
Custom	KBLU-AU		1.0
Date:	Friday, April 28, 2017		Sheet 21 of 42

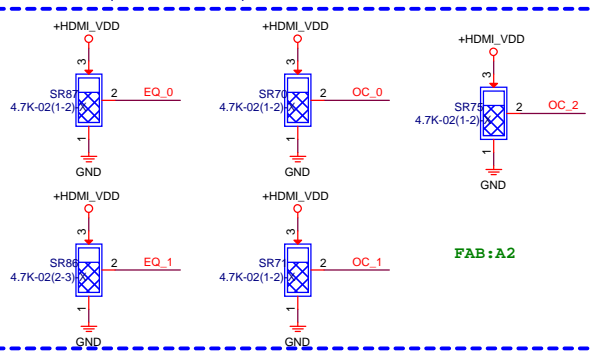
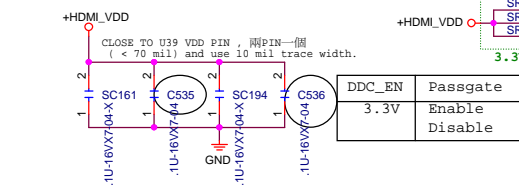
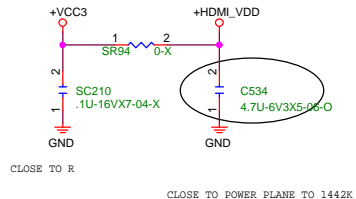
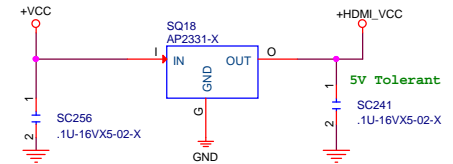


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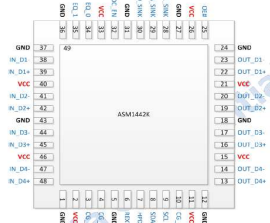
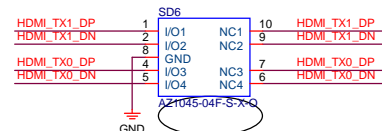
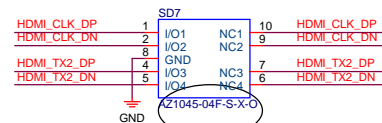
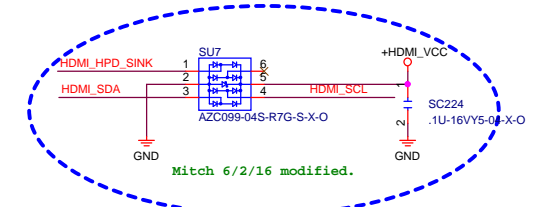
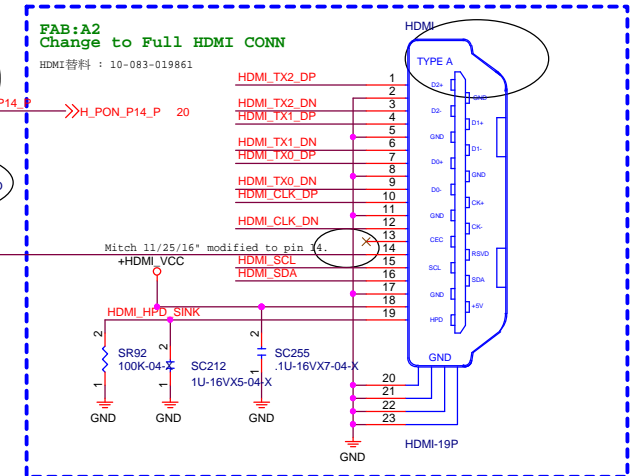
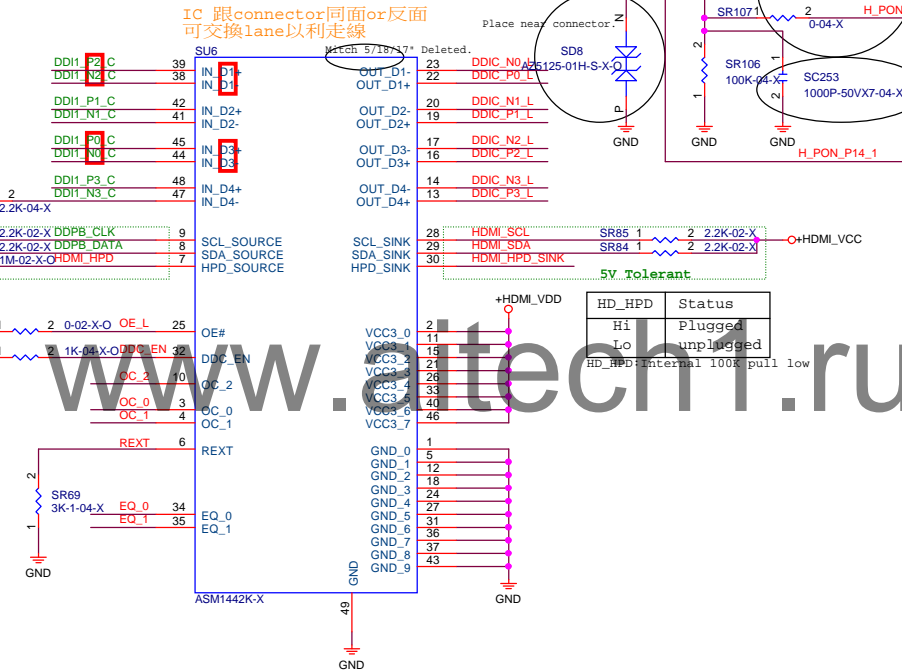


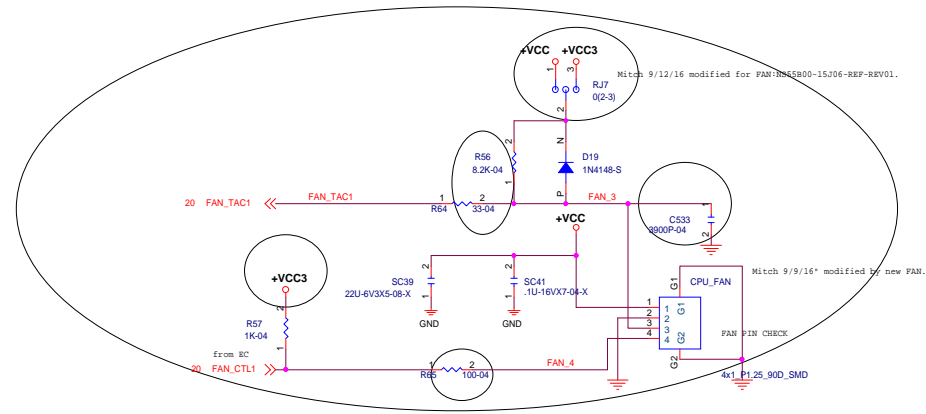
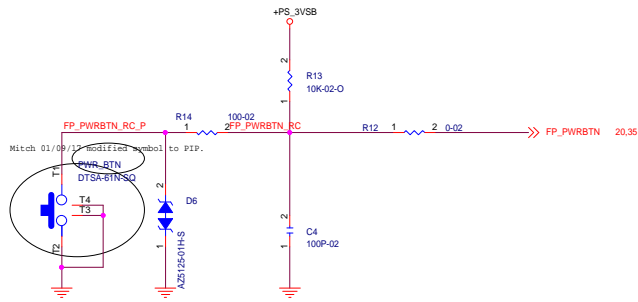
TMDS Input Signal Equalization

EQ_1	EQ_0	Equalization	Note
0	0	6dB	
0	1	3dB	
1	0	1dB	Default
1	1	0dB	

TMDS Output Signal Integrity

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note	
0	0	0	450	0	0		
0	0	1	420	0	-3dB	Shortest trace	
0	1	0	450	0	-3dB	Shortest trace	Default
0	1	1	460	0	-4dB		
1	0	0	340	0	0		
1	0	1	400	2dB	0	Longest trace	
1	1	0	400	2dB	0	Longest trace	
1	1	1	420	0	0		



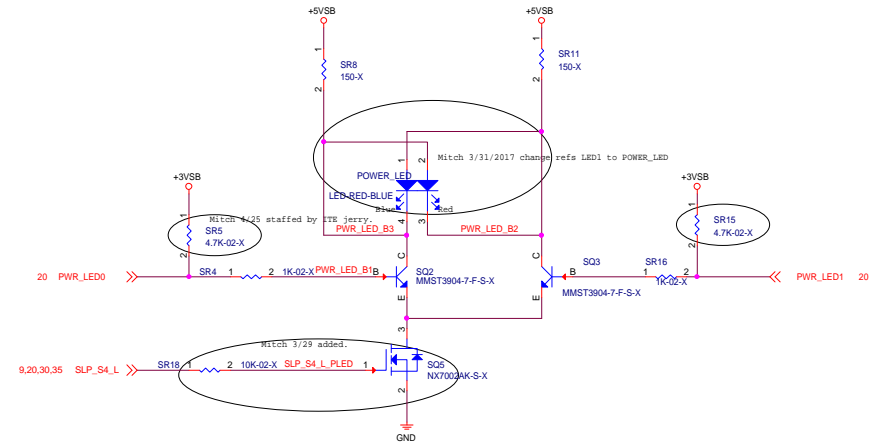


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Power LED display table:

State	LED Display
S0	ON
S3	BLINK
S4/S5/G3	OFF

Mitch 12/16/2016 deleted by ME.



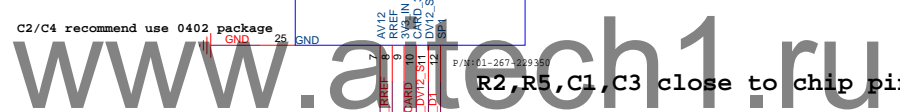
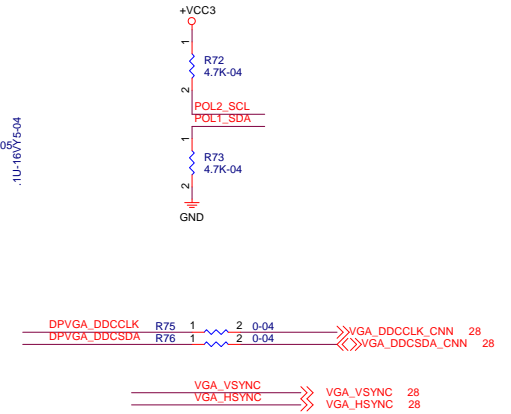
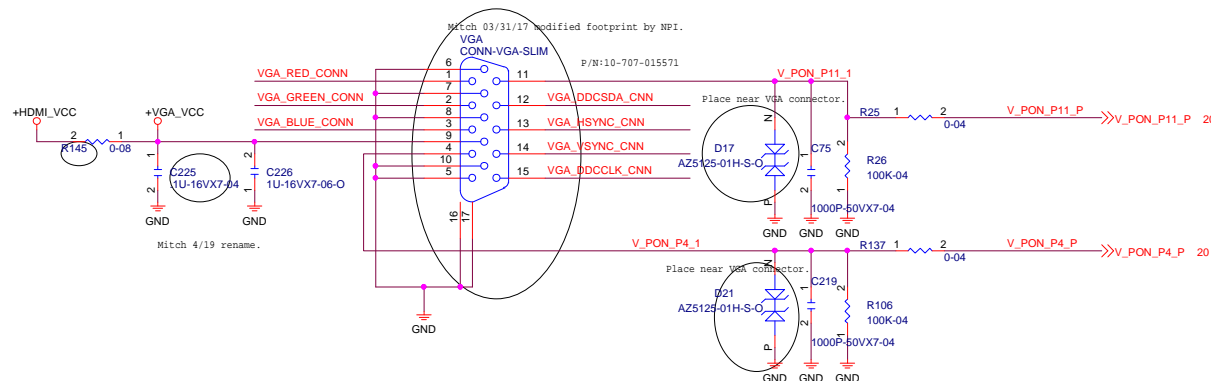
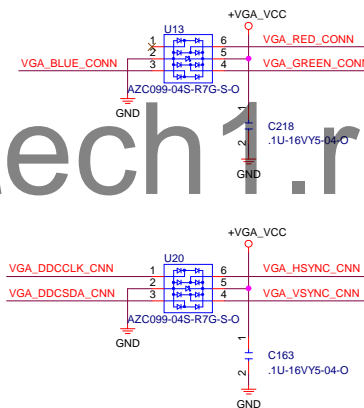
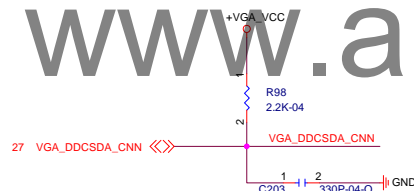
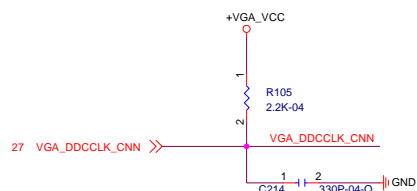
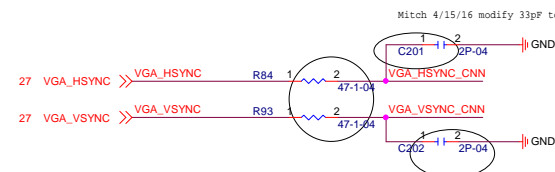
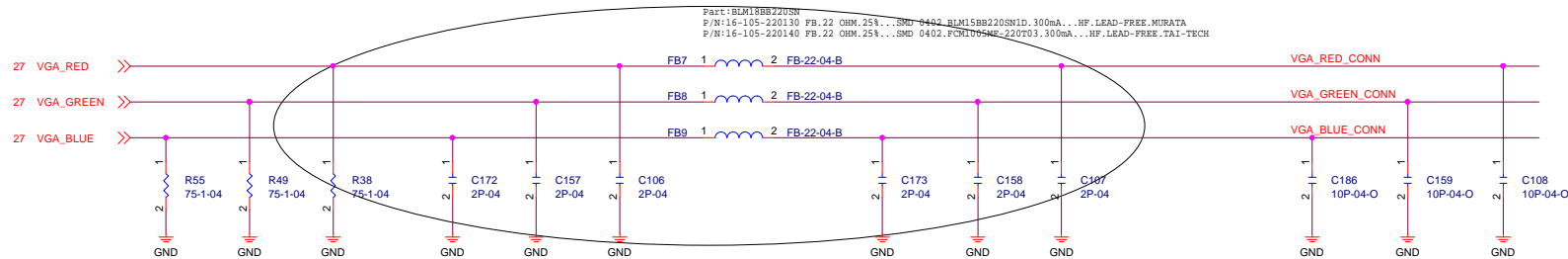


Diagram for L7: +VCC3 is connected to pin 1 of inductor L7 (FB-60-04-B), and pin 2 is connected to AVCC33.

Diagram for L5: +VCC3 is connected to pin 1 of inductor L5 (FB-60-04-B), and pin 2 is connected to VDD_DAC_33.

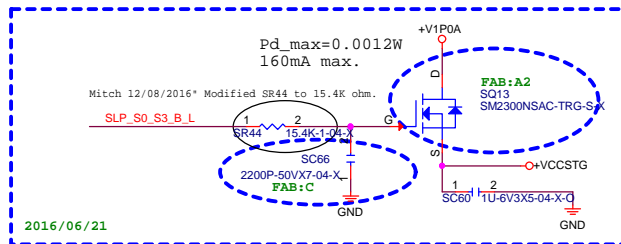
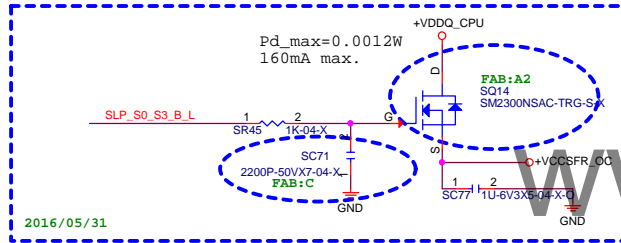
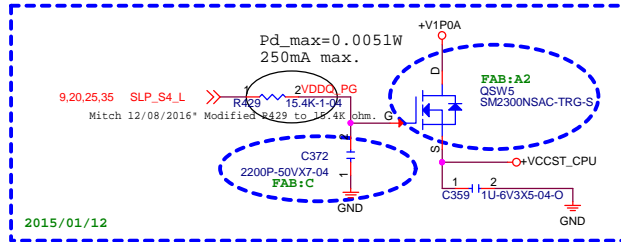
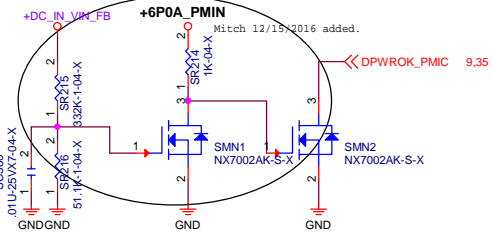
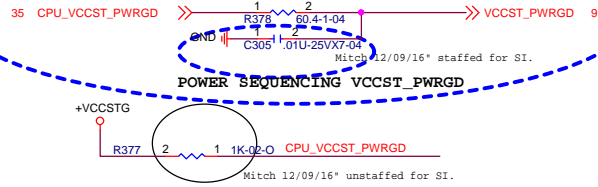


VGA

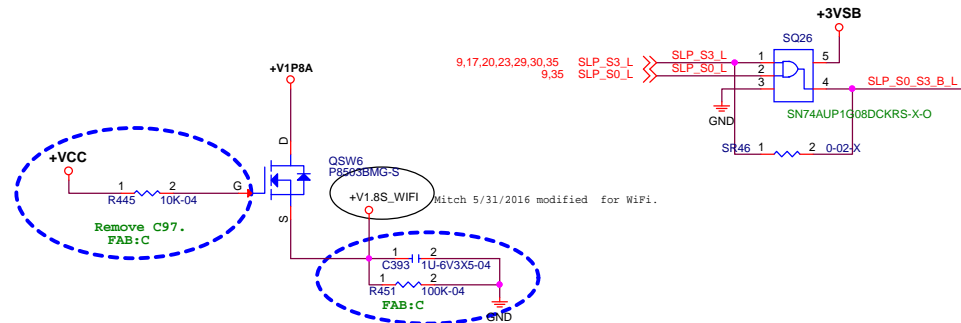
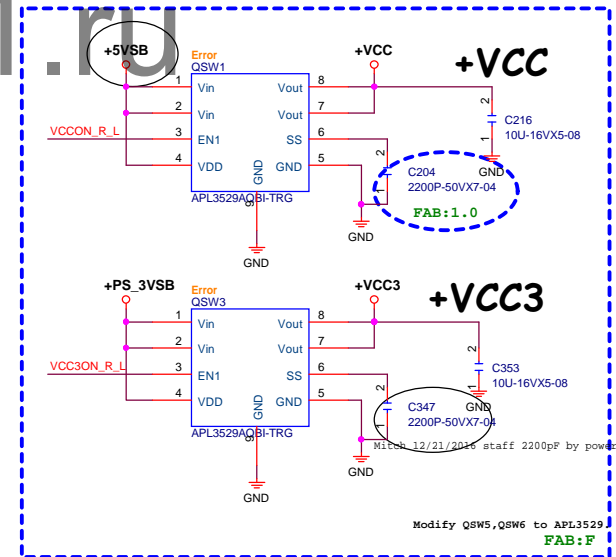
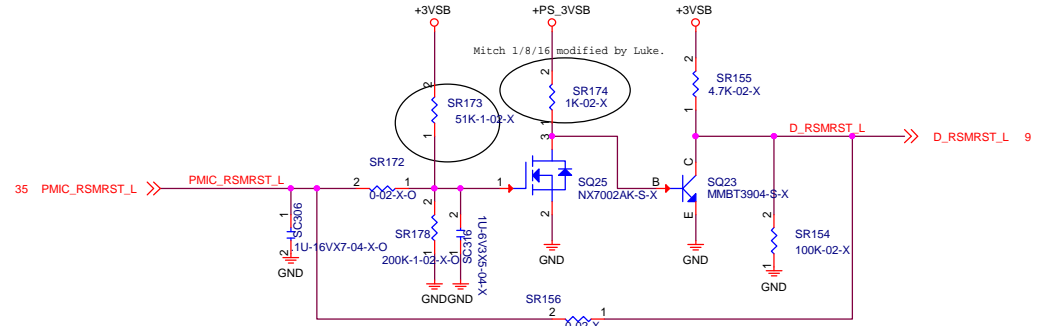
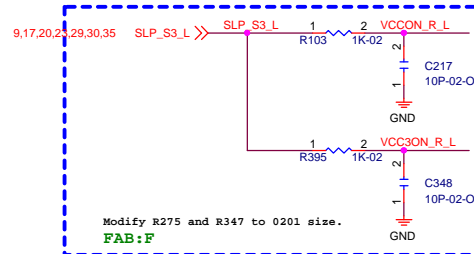


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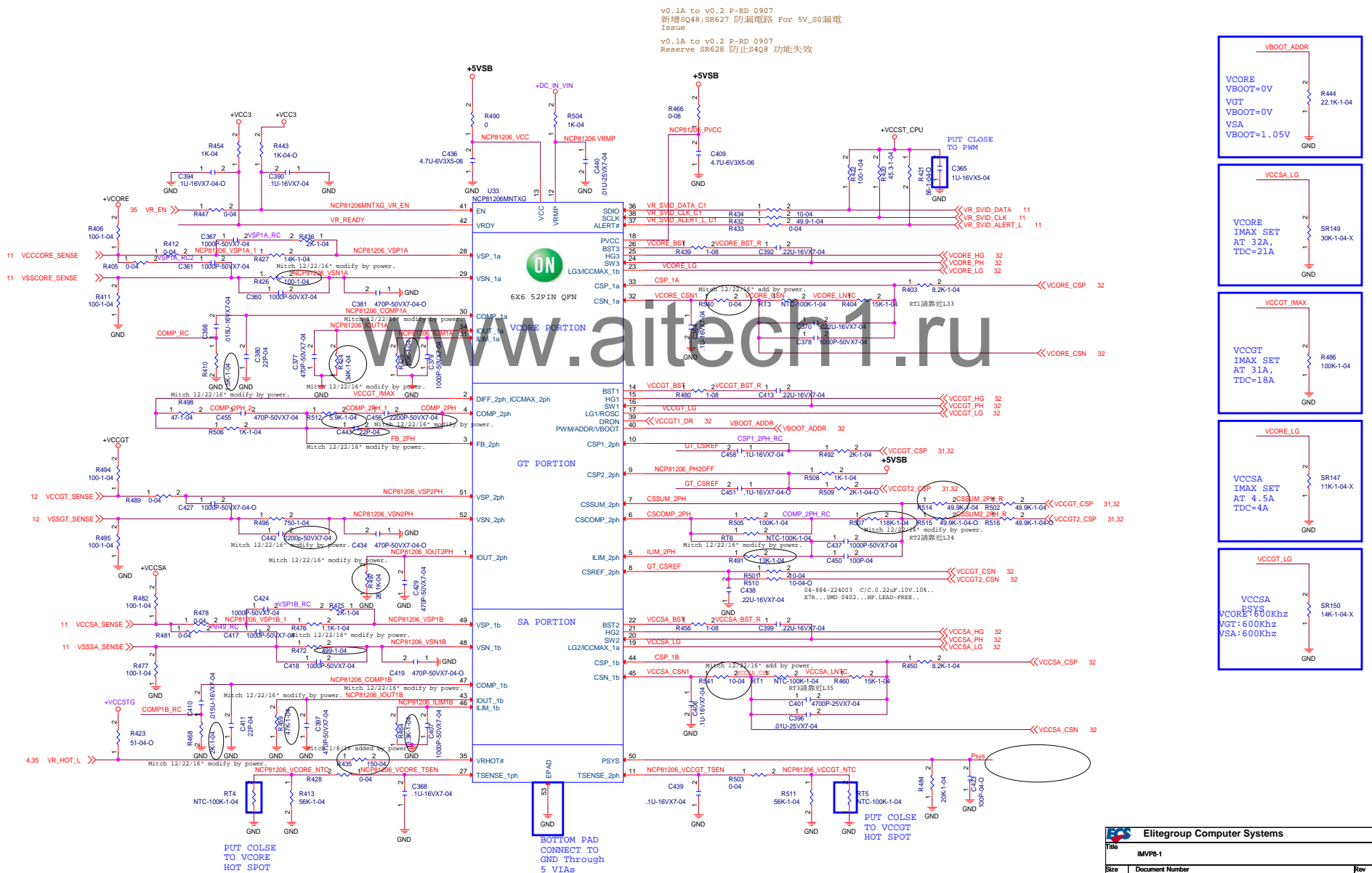
2014/10/15
Modify to 60.4 Ohm.

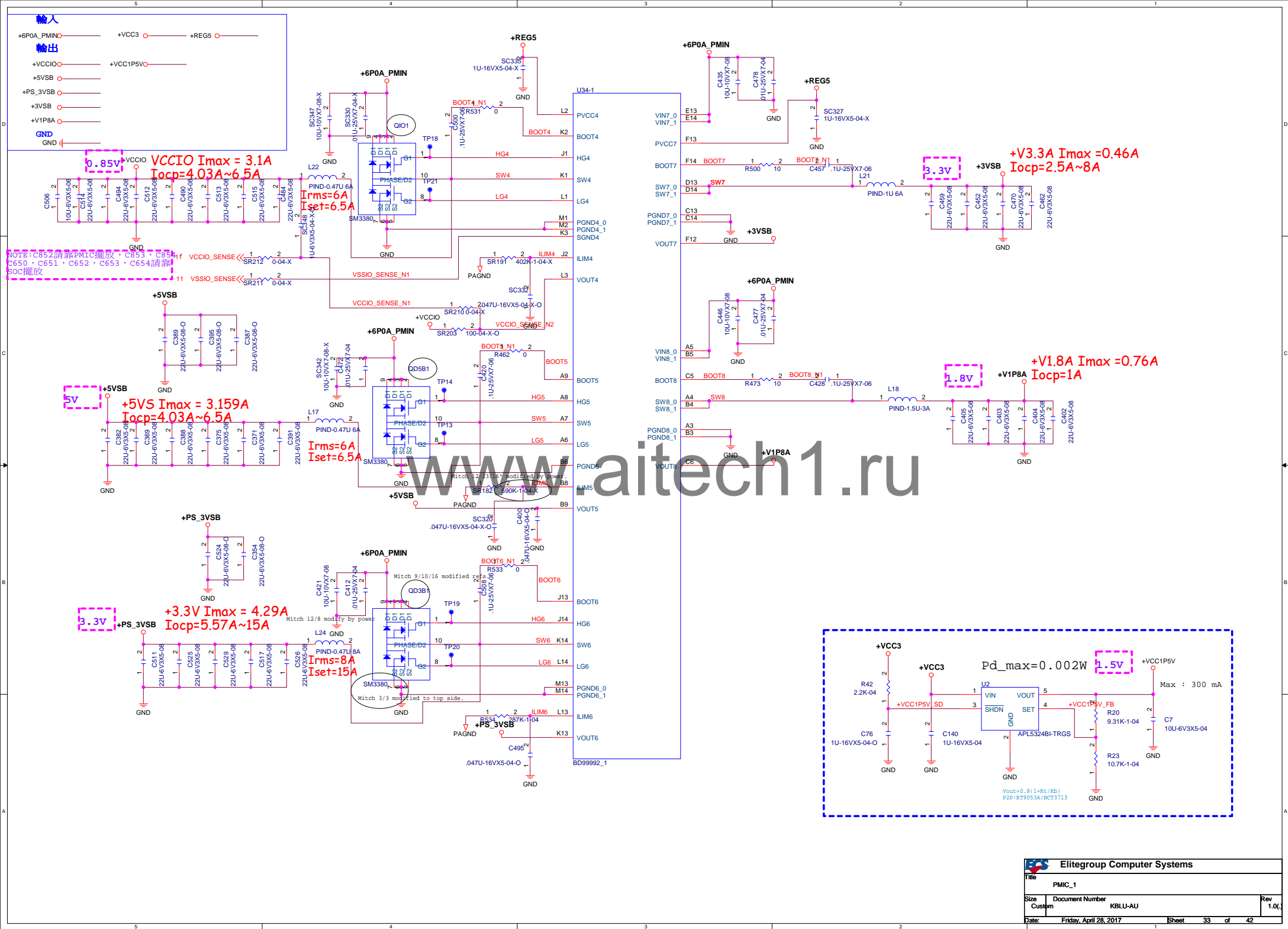


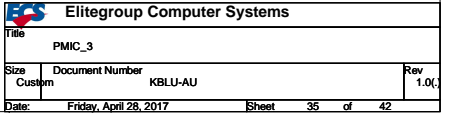
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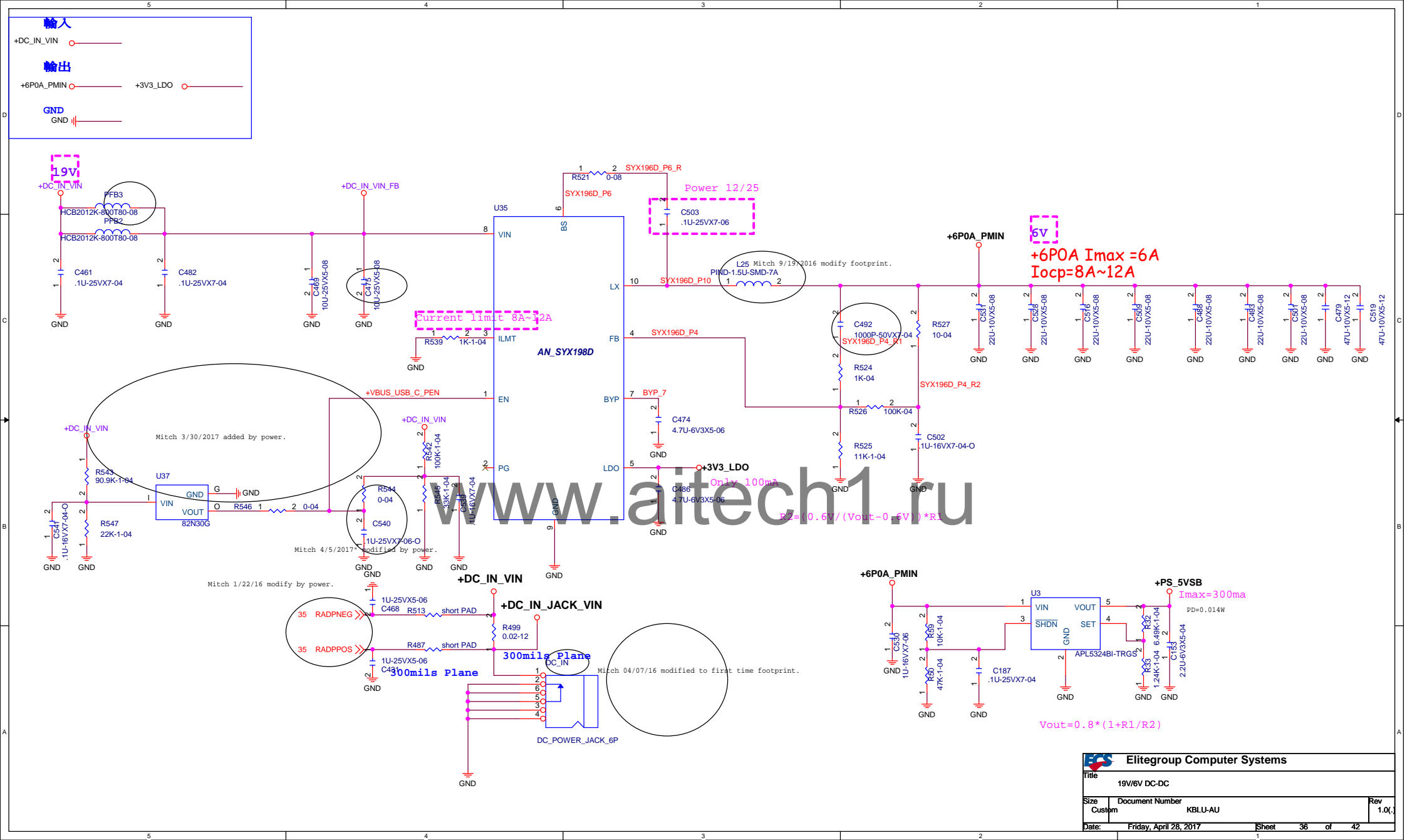


Intel SKYLAKE IMVP8 POWER









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CPU STARPPING :

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none">CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted.<ul style="list-style-type: none">1 = (Default) Normal Operation; No stall.0 = Stall.CFG[1]: Reserved configuration lane.CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.<ul style="list-style-type: none">1 = Normal operation0 = Lane numbers reversed.CFG[3]: Reserved configuration lane.CFG[4]: eDP* enable:<ul style="list-style-type: none">1 = Disabled.0 = Enabled.CFG[6:5]: PCI Express* Bifurcation<ul style="list-style-type: none">00 = 1 x8, 2 x4 PCI Express*01 = reserved10 = 2 x8 PCI Express*11 = 1 x16 PCI Express*CFG[7]: PEG Training:<ul style="list-style-type: none">1 = (Default) PEG Train Immediately following RESET# de-assertion.0 = PEG Wait for BIOS for training.CFG[19:8]: Reserved configuration lanes.	I	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PCH STARPPING_1 :

Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable "Top Swap" mode. (Default)</p> <p>1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# de-asserts.Software will not be able to clear the Top Swap bit until the system is rebooted.The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4).This signal is in the primary well.
GSP10_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable "No Reboot" mode. (Default)</p> <p>1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# de-asserts.This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after RSMRST# de-asserts.This signal is in the primary well.


PCH STARPPING_2 :

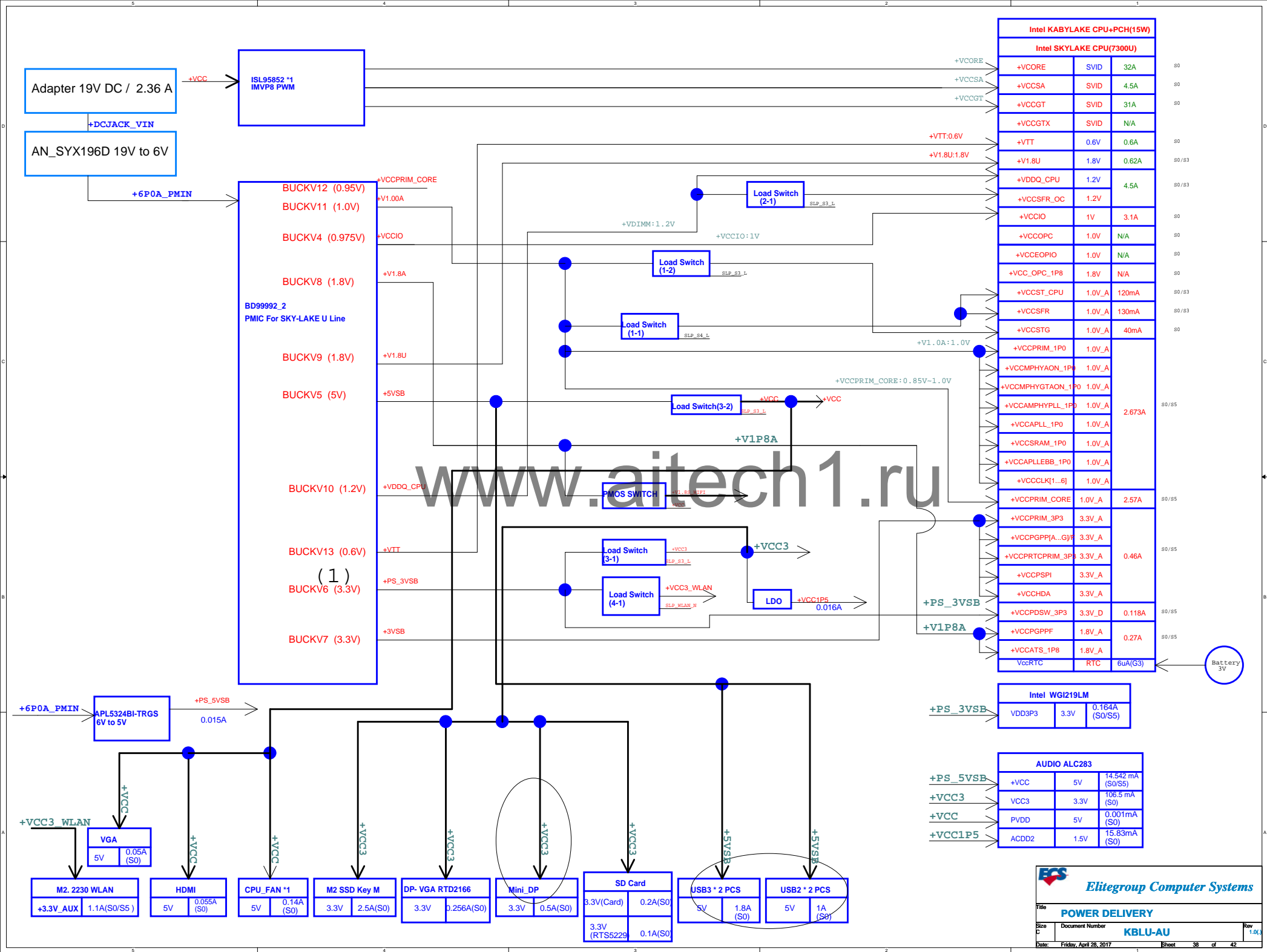
GSP11_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCH, bit 6).</p> <p>Bit 6 Boot BIOS Destination</p> <p>0 LPC (Default)</p> <p>1 SPI</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# de-asserts.If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.This signal is in the primary well.
SMLALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = LPC is selected for EC. (Default)</p> <p>1 = eSPI is selected for EC.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after RSMRST# de-asserts.This signal is in the primary well.
SP10_MOSI	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-up.</p>
SP10_MISO	Reserved	Rising edge of RSMRST#	<p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-down.</p> <p>This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p> <p>Note: When used as PCHHOT#, a 150k weak board pull-up is recommended to ensure it does not override the internal pull-down strap sampling.</p>
SP10_I02	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-up.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
SP10_I03	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-up.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>

PCH STARPPING_3 :

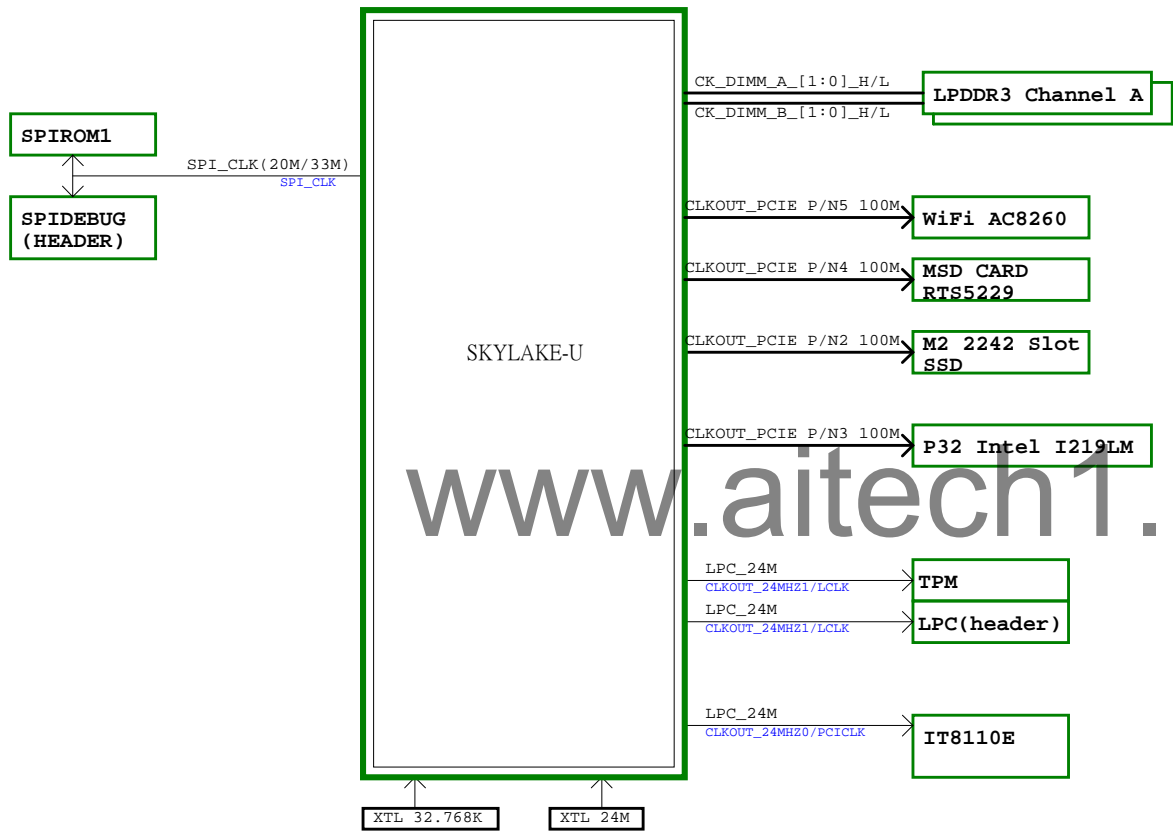
Signal	Usage	When Sampled	Comment
HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor. (Default)</p> <p>1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# de-asserts.Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.This signal is in the primary well.
DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port B is not detected. (Default)</p> <p>1 = Port B is detected.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# de-asserts.This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port C is not detected. (Default)</p> <p>1 = Port C is detected.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# de-asserts.This signal is in the primary well.

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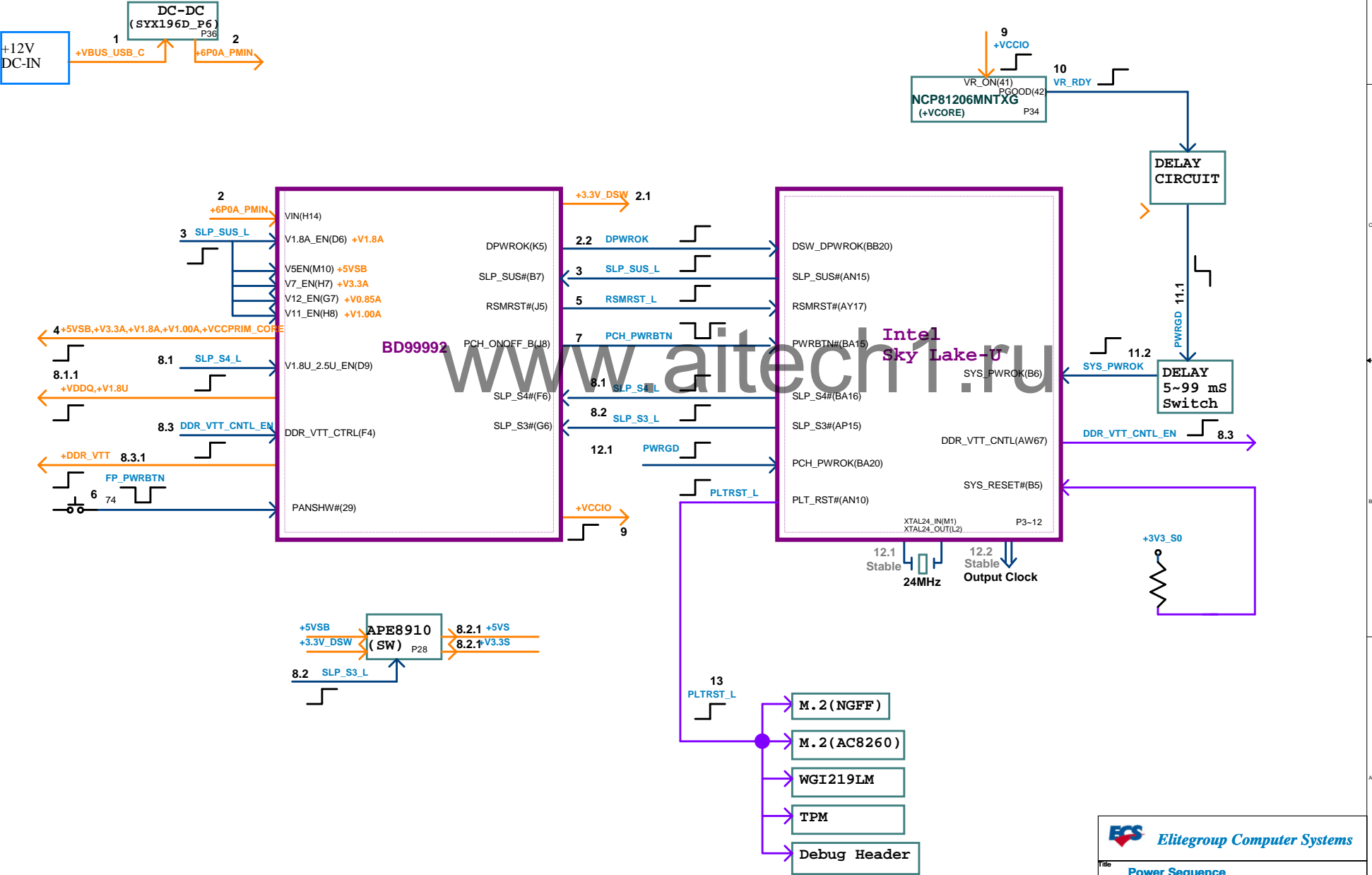
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File CPU,PCH Strapping Table	
Size Custom	Document Number KBLU-AU Rev 1.0
Date Friday, April 28, 2017 Sheet 37 of 42	



CLK Distribution

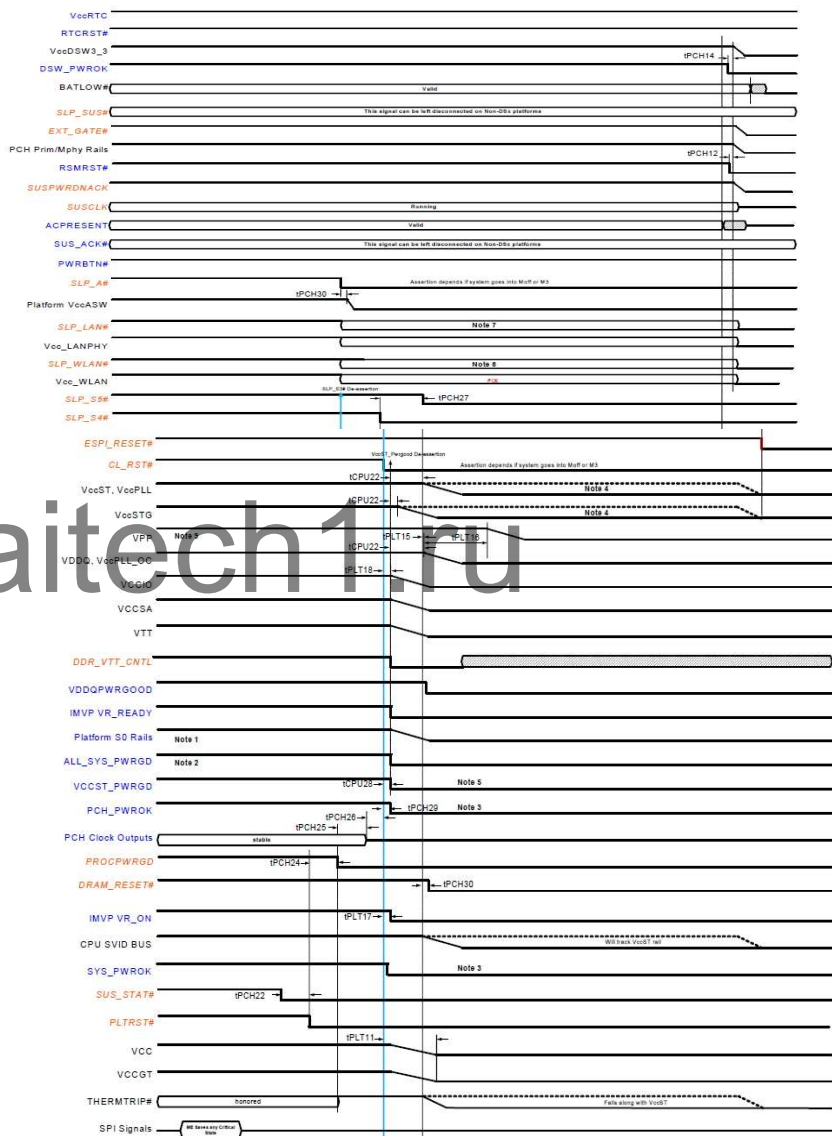
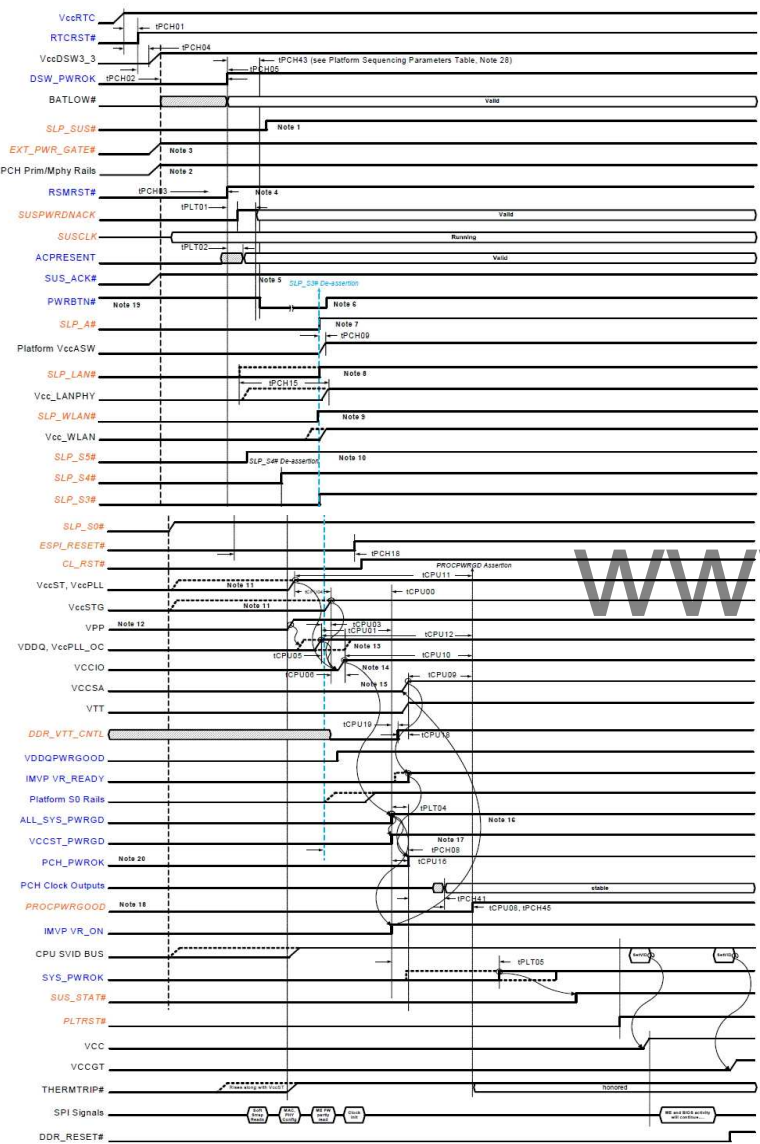


PWR Sequence & RST Diagram



Power On Sequence

Power Off Sequence



Schematics Version History Table :

Rev.	Date	Note
A3	5/31/2016	Initial modified schematic.
A4	11/24/2016	Modify power by HDMI circuit. M2.PCIE/SATA select circuit.24/25Mhz value of cap.
A4/A5	01/06/2017	Change version from VB to 1.0 for PM request.
A4/A5	03/31/2017	Change version from V1.0 to 1.0.for PM request. To fix clear CMOS button and DC plug in 6V PWM power off issue
A4/A5	05/18/2017	Delete "Error" message on LAN chip, Lan connector, Audio jack, LAN transformer , M2 SSD slot.

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